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LVCMOS Based Energy Efficient Sindhi Unicode Reader for Natural Processing on 28nm FPGA

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Abstract

In this research work, we have focused on designing an energy efficient Sindhi Unicode reader based on LVCMOS for natural processing. Unicode is a standard for a universal character set for all the scripts of the world. It is one of the fundamental technological building blocks for exchanging textual information internationally, via computers. The scripts of Sindh are Brahmi-based writing systems. Our main aim of this paper is to build an energy efficient low power design for this we have taken different frequencies and calculated its power. We have done power analysis on a constant temperature that is 25 degree Celsius and also keeping air flow constant. We have varied frequency and calculated power for different LVCMOS IO STANDARDs. Our design is based on 28nm FPGA and the code has been tested on Kintex-7 and the device used is XC7K160T, package used is FBG676 and it is working on -3 speed grade. At the end we have concluded that there is 3.27%, 3.38%, 4.34%, 3.12%, 4.54%, 4.28% saving in power dissipation with LVCMOS18 and LVCMOS15 when compared with LVCMOS33 at 1400 MHz, 1.2 GHz, 2100 MHz, 1700 MHz, 1800MHz, 2.2 GHz respectively.

Keywords: *LVCMOS, Unicode Reader, FPGA, energy efficient, Sindhi*

1. Introduction

India is Multilingual Multi script Country [1]. Indian languages are originated from Sanskrit [1]. Indic scripts have originated from Brahmi script [1]. The scripts of Sindh are Brahmi-based writing systems [2]. These scripts were used throughout Sindh for writing Sindhi and other Indo-Aryan languages [2]. Unicode is known as the "Universal Alphabet", which is actually an ordered set of 216, *i.e.,* 65536 characters that covers the majority of scripts or writing systems existing in the world. Unicode is a standard for a universal character set for all the scripts of the world. It is one of the fundamental technological building blocks for exchanging textual information internationally, via computers [8]. There is a wide research gap to design energy efficient hardware designs which is nowadays in use in text analysis [3]. In this research work, we have designed a Sindhi Unicode Reader that will translate Sindhi Language into other languages and will tell us about the consonants, vowels, numerals, honorifics special signs, punctuations present at the input of the Unicode reader. A lot of research has been done in the field of Unicode readers and many researches have presented their work and are still working for better results. Comparison between the two languages that is Arabic and Punjabi has been done [4]. Paper discusses additions to Arabic Script for the representation of Punjabi

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language [4]. Other researchers have designed thermal aware Bengali Unicode reader [3], post-processor for Gurmukhi OCR [5] and Online Handwritten Gurmukhi Words Recognition [6] and low power Devnagari Unicode reader [7] too. Our design has been operated at 25 degree Celsius and at different operating frequencies mentioned in Table. 3. As mentioned earlier, India is Multilingual Multi script Country. Indian scripts are famous all over the world. Table 1 shows the Unicode range of 8 different Indian scripts.

Table 1. Range of Some Indian Language Unicode Scripts

		Script
0x0900	0x097F	Devnagari
0x0980	0x09FF	Bengali/Assamese
0x0A01	0x0A75	Gurumukhi
0x0A80	0x0AFF	Gujarati
0x0B00	0x0B7F	Oriya
0x0C00	0x0C7F	Telugu
0x0C80	0x0CFF	Kannada
0x0D00	0x0DFF	Malayalam

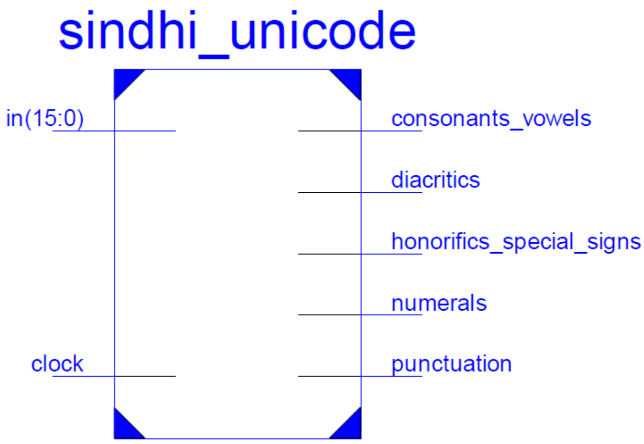

Figure 1. Symbol of Sindhi Unicode Reader

The schematic of Sindhi reader takes 16-bit hexadecimal code of alphabet and clock input as shown in Figure 1. The output that can be given by this reader can be one of five outputs. Depending on the type of Sindhi input, the output will be at the corresponding port as shown in Figure 1. Sindhi Unicode takes input as an alphabet and gives corresponding output like consonants, vowels, diacritics, honorifics special signs, numerals, punctuation.

Table 2. Different Parameters in Kintex-7 FPGA

IO pins	676
LUT Elements	101400
Flip Flop	202800
DSPS	600
Available IOBS	400
Gb transceiver	8
Block RAM	325
GTXE2 Transceiver	8
PCI Buses	1.1
MMCMS	8

Min operating temperature	0 degree Celsius
Reference operating temperature	85 degree Celsius
Maximum operating Temperature	85 degree Celsius
Minimum operating voltage	0.97V
Reference operating Voltage	0.97V
Maximum operating Voltage	1.03V
Temperature Grade Letter	C

Our design is based on 28nm FPGA and the code has been tested on Kintex-7 and the device used is XC7K160T, package used is FBG676 and it is working on -3 speed grade. Table 2 shows different parameters in kintex-7 FPGA. XPower Analyzer is used for power analysis. LVMOS25 logic family is used for impedance matching of transmission line, device and port.

Table 3. Set of Frequencies Taken in Consideration

Frequency	**Mobile set**
1400MHz	Nokia Lumia 710
1.2GHz	Samsung Galaxy Core
2100MHz	I phone6
1700MHz	HTC/T
1800MHz	Micromax X091
2.2GHz	Sony Xperia Z1

4. Power Analysis

A. Power Analysis for LVCMOS18 IO STANDARD

Table 4. Power Analysis for LVCMOS18 IO STANDARD

FREQUENCY	POWER
1400 MHz	0.059
1.2 GHz	0.057
2100 MHz	0.066
1700 MHz	0.062
1800 MHz	0.063
2.2 GHz	0.067

There is 14.92% saving in total power dissipation with 1.2 GHz when compared with 2.2GHz as shown in Figure 2 and Table 4.

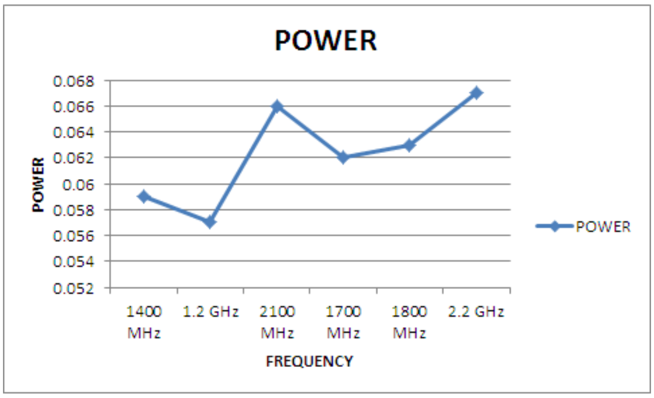

Figure 2. Power Analysis for LVCMOS18 IO STANDARD

B. Power Analysis for LVCMOS33 IO STANDARD

Table 5. Power Analysis for LVCMOS33 IO STANDARD

FREQUENCY	POWER
1400 MHz	0.061
1.2 GHz	0.059
2100 MHz	0.069
1700 MHz	0.064
1800 MHz	0.066
2.2 GHz	0.070

There is 15.71% saving in total power dissipation with 1.2 GHz when compared with 2.2GHz as shown in Figure 3 and Table 5.

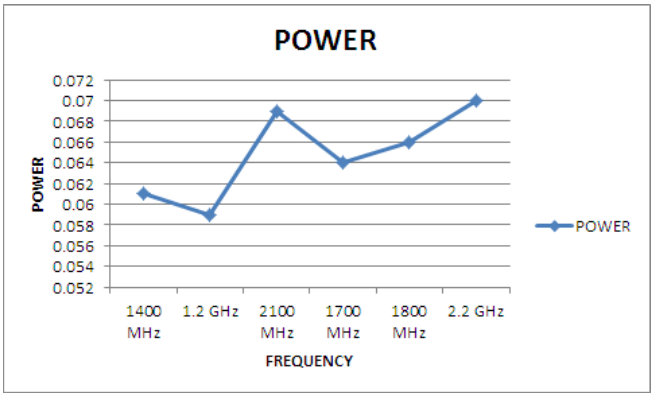

Figure 3. Power Analysis for LVCMOS33 IO STANDARD

C. Power Analysis for LVCMOS25 IO STANDARD

Table 6. Power Analysis for LVCMOS25 IO STANDARD

FREQUENCY	POWER
1400 MHz	0.060
1.2 GHz	0.058
2100 MHz	0.067
1700 MHz	0.063
1800 MHz	0.064
2.2 GHz	0.068

There is 14.70% saving in total power dissipation with 1.2 GHz when compared with 2.2GHz as shown in Figure 4 and Table 6.

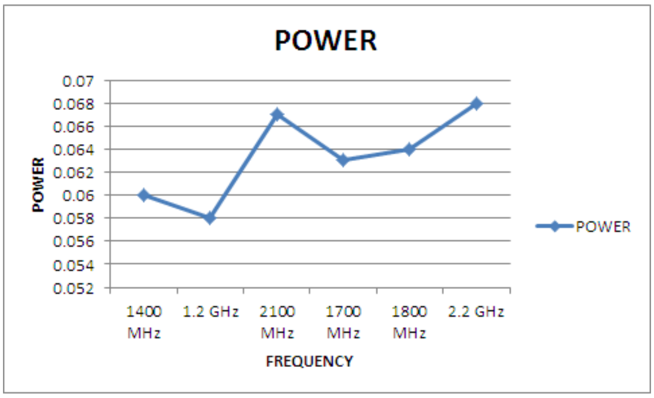

Figure 4. Power Dissipation for LVCMOS25 IO STANDARD

D. Power Analysis for LVCMOS15 IO STANDARD

Table 7. Power Analysis for LVCMOS15 IO STANDARD

FREQUENCY	POWER
1400 MHz	0.059
1.2 GHz	0.057
2100 MHz	0.066
1700 MHz	0.062
1800 MHz	0.063
2.2 GHz	0.067

There is 14.92% saving in total power dissipation with 1.2 GHz when compared with 2.2GHz as shown in Figure 5 and Table 7.

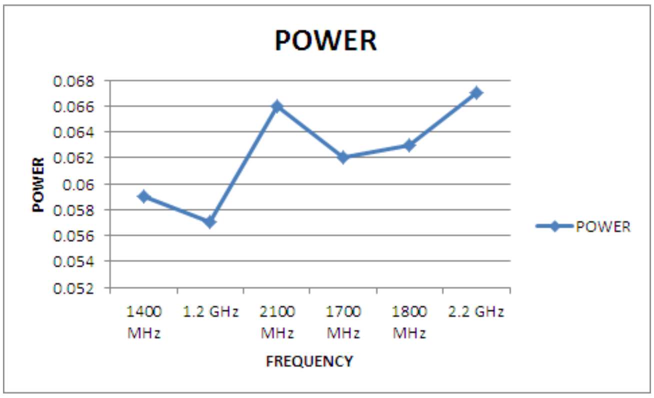

Figure 5. Power Analysis for LVCMOS15 IO STANDARD

E. Power Analysis for different IO STANDARD with Different Frequencies

Table 8. Power Analysis for LVCMOS Family at Different Frequencies

IO STANADARD	1400 MHz	1.2 GHz	2100 MHz	1700 MHz	1800 MHz	2.2 GHz
LVCMOS18	0.059	0.057	0.066	0.062	0.063	0.067
LVCMOS33	0.061	0.059	0.069	0.064	0.066	0.070

LVCMOS25	0.060	0.058	0.067	0.063	0.064	0.068
LVCMOS15	0.059	0.057	0.066	0.062	0.063	0.067

There is 3.27%, 3.38%, 4.34%, 3.12%, 4.54%, 4.28% saving in power dissipation with LVCMOS18 and LVCMOS15 when compared with LVCMOS33 at 1400 MHz, 1.2 GHz, 2100 MHz, 1700 MHz, 1800MHz, 2.2 GHz respectively as shown in Figure 6 and Table 8.

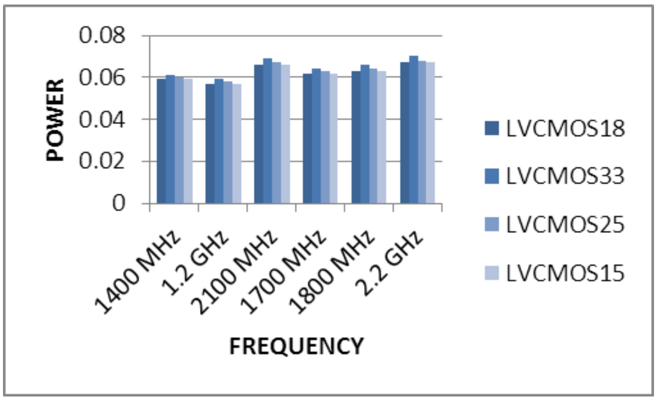

Table 6. Power Analysis for LVCMOS Family at Different Frequencies

3. Conclusion

There was research gap in natural language processing for energy efficient design. Here, by designing the energy efficient Sindhi Unicode Reader we have filled this research gap. This Unicode reader code has been implemented on Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform using Kintex-7 FPGA family. The device has been designed to convert Sindhi language into different languages that our people could understand. Our Unicode reader is operating at 25 degree Celsius. The design is LVCMOS based and is tested at various operating frequencies such as 1400 MHz, 1.2 GHz, 2100 MHz, 1700 MHz, 1800 MHz, 2.2GHz. This is an energy efficient device because there is 3.27%, 3.38%, 4.34%, 3.12%, 4.54%, 4.28% saving in power dissipation with LVCMOS18 and LVCMOS15 when compared with LVCMOS33 at 1400 MHz, 1.2 GHz, 2100 MHz, 1700 MHz, 1800MHz, 2.2 GHz respectively.

4. Future Scope

The future scope of “LVCMOS Based Energy Efficient Sindhi Unicode Reader for Natural Processing on 28nm FPGA” is that we can also implement this design on 22nm or 18 nm FPGA. We can also use different FPGA families like automotive Artix7, automotive Coolrunner2, automotive Spartan, automotive Spartan-3A DSP, automotive Spartan 3A, automotive Spartan 3E, automotive Spartan6, Spartan3, Spartan3E. Here, we are using frequency scaling in which we are changing the operating frequency of a device and analyzing its power. We can redesign this unicode reader with other energy efficient technique like capacitance scaling, thermal scaling, clock gating, various design goals, impedance matching with different logic family, and mapping. Analysis has been done with different frequencies like 1400 MHz, 1.2 GHz, 2100 MHz, 1700MHz, 1800MHz, 2.2GHz. We can use any other frequency range and test our design on that also. The temperature has been kept constant that is 25 degree Celsius so if needed it can also be varied. Air flow can also be varied when required.

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