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Capacitance Scaling Based Energy Efficient and Tera Hertz Design of Malayalam Unicode Reader on FPGA

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Abstract

Malayalam is Kerala's official language, south-western region of India mainly speak this language, and very less research has been done for designing Malayalam Unicode reader. The Unicode range of characters for Malayalam script is 0D00–0D7F. In this work, we are focusing on the script of Malayalam language and its Unicode required for coding in Hardware Descriptive Language. This paper covers the hardware design and implementation of Malayalam Unicode Reader (MUR) for Kairali scripts on Virtex-6 FPGA. This MUR design was tested with the device operating at frequency of 1THz, Capacitance has been varied from 1pF to 25pF with SSTL family (Stub Series Terminated Logic) with an interval of 5pf.

Keywords: *Malayalam Unicode Reader, Unicode, SSTL, IO Standard, Energy Efficient Hardware design, FPGA*

1. Introduction

Malayalam (/malayALam/) main language of Kerala (South India) & the Lakshadweep Islands (Laccadives) (west coast of India) [1]. Malayalis (speakers of Malayalam) are almost totally literate. 4 % of the population of India speaks Malayalam and 96% of the population of Kerala speaks it (29.01 million in 1991). [1] Malayalam ranks 8 among the 15 major languages of India. The great majority of residents of Kerala are Malayalis, but there are many smaller ethnic groups including Tuluvas, Tamils, Kannadigas and Konkanis. Malayalam Vowels have unique and independent symbol. Malayalam language has 38 consonants [2]. Consonants also have symbols for them. Different symbols have been used for vowels and consonants. This Unicode reader can count the number of vowel, consonants, and digit when used with counter. Different Unicodes have been developed for different symbols with a range of 0x0D00 to 0x0DFF [2]. For implementation of Malayalam Unicode reader, we have used different IO standards of SSTL (Stub Series Terminated Logic) named as SSTL18_I, SSTL18_II, SSTL2_II_DCI & SSTL18_II_DCI were used. Capacitance scaling technique had already been used in the Gurmukhi Unicoder [3.] We analyzed the power changes at 1THz frequency while varying capacitance from 1pF to 25 pF with an interval of 5pf. Frequency scaling can also be done by keeping the capacitance constant for different frequencies [4]. Thermal aware energy efficient design can also be made by varying the heat sink and airflow [5]. Output load can also be varied to make the device energy and power efficient [6].Clock gating is also one of the power efficient technique which can be used to make the power efficient design and can contribute to green communication [7]. Different logic

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families can also be used to make the device more ecofriendly [8]. Techniques like voltage and frequency scaling can also make the energy efficient devices [9, 10]. Various Computer, and Solar devices can also be made energy and power efficient by using different design techniques [11, 12].

Table 1: Range Allocation for Some Indian Unicode Scripts [2]

Hexadecimal Range		Script
0x0900	0x097F	Devnagari
0x0980	0x09FF	Bengali/Assamese
0x0A00	0x0A7F	Gurumukhi
0x0A80	0x0AFF	Gujarati
0x0B00	0x0B7F	Oriya
0x0C00	0x0C7F	Telugu
0x0C80	0x0CFF	Kannada
0x0D00	**0x0DFF**	**Malayalam**

Table drawn above shows the various Unicode ranges for different language scripts. Within this Unicode Script range one can frame a program in hardware descriptive language. All vowels and consonants are included in Unicode script range Range for MALAYALAM SCRIPT lies in the range between 0x0D00 upto 0x0DFF.

2. Experimental Set-Up

This design was implemented on Virtex-6 FPGA family with Xilinx ISE 13.2 simulator and Verilog HDL (hardware description language). X Power Analyzer was used for power analysis and the values of capacitances was varied at output load from 1pf to 25 pf. SSTL logic family was used for impedance matching of transmission line, device and port. Basic elements(BELS) used were 16 out of which 1 LUT3, 2 LUT4, 2 LUT5, 9 LUT6, 1 MUXF7, 1 Clock Buffers, 22 IO Buffers(IBUF:16,OBUF:6), 5 Flip Flops were being used. X Power Analyzer was being used for power analysis. Number of Slice Registers: 5 out of 93120, number of Slice LUTs: 14 out of 46560 were being used.23 Numbers of IOs out of 240.

A. Schematic of Malayalam Unicode Reader

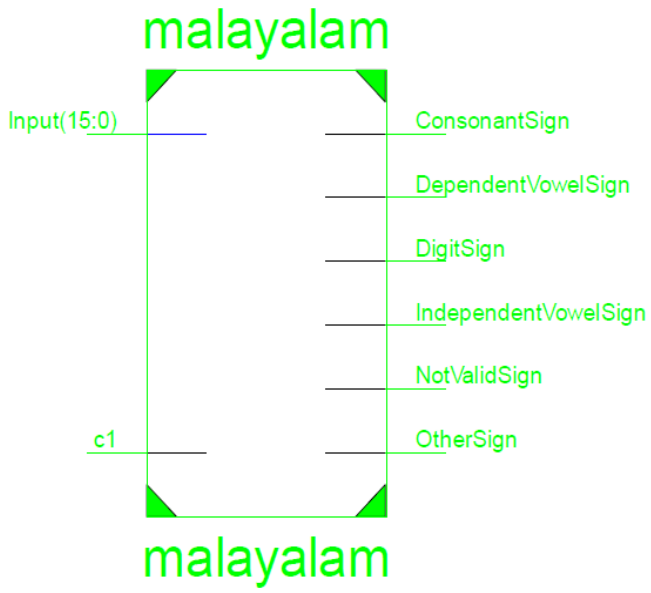


Figure 1. Schematic of Malayalam Unicode Reader

The schematic of Malayalam reader has 16-bit hexadecimal code for alphabet along with a clock input as shown in Figure1.There are six outputs for the schematic, output can be observed at any of the six output pins given by this reader. Non valid sign output will only be activated, when any symbol doesn't lie in the range of Malayalam Unicode. Each output depends on Malayalam input.

3. Results

A. Power Dissipation of Unicode Reader on SSTL18_I

Table 2. IO Power Dissipation for Different Output Load on SSTL18_I

Capacitance Scaling at frequency of 1 THz and IO standard SSTL18_I						
Capacitance→ Power↓	1pf	5pf	10pf	15pf	20pf	25pf
Clock	16.211	16.211	16.211	16.211	16.211	16.211
Logic	0.0165	0.016	0.016	0.016	0.0165	0.0165
Signals	1.450	1.450	1.450	1.450	1.450	1.450
IOs	15.045	15.317	15.657	15.997	16.337	16.676
Leakage	1.028	1.028	1.028	1.028	1.028	1.028
Total	33.750	34.022	34.362	34.702	35.042	35.382

When the capacitances were scaled from 1pf to 25pf with an interval of 5pf using SSTL18_I**, 9.780522%** I/O power was being saved if we works at 1pf instead of 25pf,8.145% power is being saved if we works at 5pf instead of 25pf,6.11% I/O power was being saved if we works at 10pf instead of 25pf, 4.0717% I/O power was being saved if we works at 15pf instead of 25pf, 2.032% I/O power was being saved if we works at 20pf instead of 25pf.There is no change in all the other powers inspite of IO power if we do capacitive scaling from 1pf to25pf.

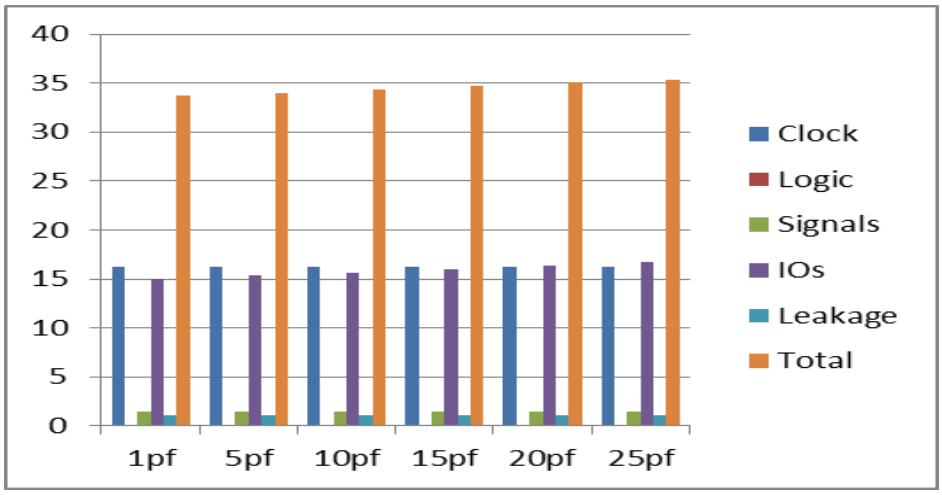


Figure 2. IOs Power (mW) Versus Output Load (pF)

B. Power Dissipation of Unicode Reader on SSTL18_II

Table 3. IO Power Dissipation for Different Output Load

Capacitance Scaling at frequency of 1 THz and IO standard SSTL18_II						
Capacitance→ Power↓	1pf	5pf	10pf	15pf	20pf	25pf
Clock	16.211	16.211	16.211	16.221	16.221	16.221
Logic	0.016	0.016	0.016	0.016	0.016	0.016
Signals	1.450	1.450	1.450	1.450	1.450	1.450
IOs	18.684	19.155	19.743	20.332	20.920	21.508
Leakage	1.028	1.028	1.028	1.028	1.028	1.028
Total	37.389	37.860	38.488	39.037	39.625	40.214

When the capacitances were scaled from 1pf to 25pf with an interval of 5pf using SSTL18_II, **13.122%** I/O power was being saved if we works at 1pf instead of 25pf,10.940% power is being saved if we works at 5pf instead of 25pf,6.11% I/O power was being saved if we works at 10pf instead of 25pf, 8.20% I/O power was being saved if we works at 15pf instead of 25pf, 2.733% I/O power was being saved if we works at 20pf instead of 25pf.There is no change in all the other powers inspite of IO power if we do capacitive scaling from 1pf to 25pf.

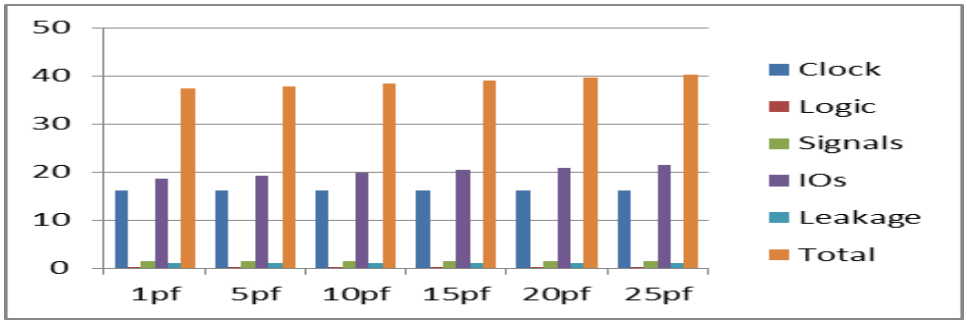


Figure 3. IOs Power (mW) Versus Capacitance Output Load (pF)

C. Power Dissipation of Unicode Reader on SSTL2_II_DCI

Table 4. IO Power Dissipation for Different Output Load

Capacitance Scaling at frequency of 1 THz and IO standard SSTL2_II_DCI						
Capacitance→ Power↓	1pf	5pf	10pf	15pf	20pf	25pf
Clock	16.211	16.211	16.211	16.221	16.221	16.221
Logic	0.016	0.016	0.016	0.016	0.016	0.016
Signals	1.450	1.450	1.450	1.450	1.450	1.450
IOs	15.083	16.200	17.595	18.991	20.386	21.503
Leakage	1.029	1.029	1.029	1.029	1.029	1.029
Total	33.789	34.906	36.301	37.697	39.029	40.209

When the capacitances were scaled from 1pf to 25pf with an interval of 5pf using SSTL2_II_DCI, **29.885%** I/O power was being saved if we works at 1pf instead of 25pf,24.66% power is being saved if we works at 5pf instead of 25pf,18.742% I/O power was being saved if we works at 10pf instead of 25pf, 11.68% I/O power was being saved if we works at 15pf instead of 25pf, 5.914% I/O power was being saved if we works at 20pf instead of 25pf.There is no change in all the other powers inspite of IO power if we do capacitive scaling from 1pf to 25pf.

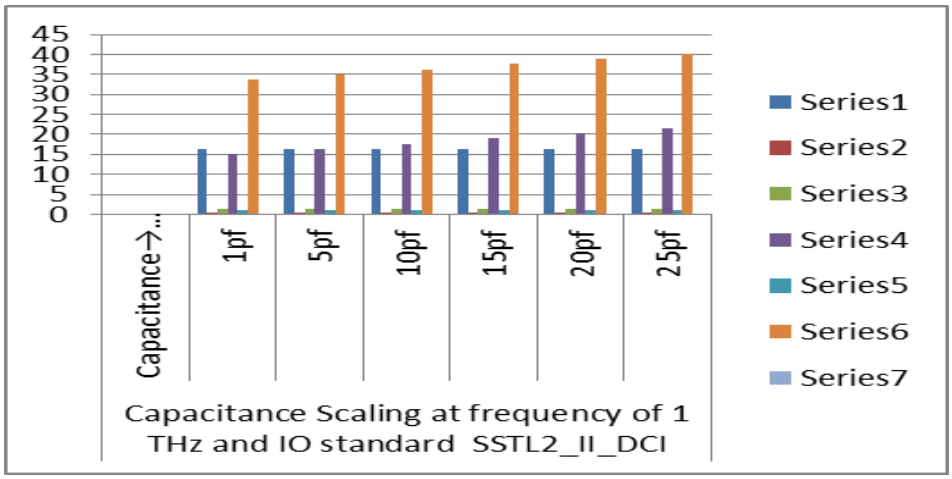


Figure 3. IOs Power (mW) Versus Output Load (pF)

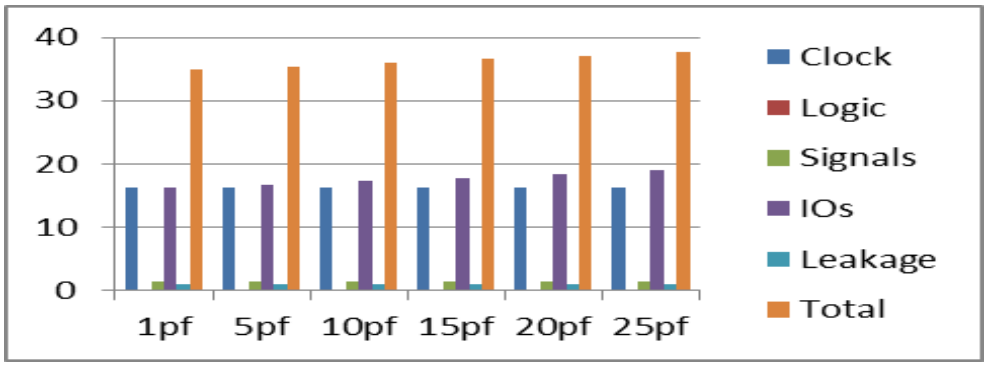
D. Power Dissipation of Unicode Reader on SSTL18_II_DCI

Table 4. IO Power Dissipation for Different Output Load SSTL18_II_DCI

Capacitance Scaling at frequency of 1 THz and IO standard SSTL18_II_DCI						
Capacitance→ Power↓	1pf	5pf	10pf	15pf	20pf	25pf
Clock	16.211	16.211	16.211	16.221	16.221	16.221
Logic	0.016	0.016	0.016	0.016	0.016	0.016
Signals	1.450	1.450	1.450	1.450	1.450	1.450
IOs	16.188	16.659	17.247	17.836	18.424	19.013
Leakage	1.028	1.028	1.028	1.028	1.028	1.028
Total	34.893	35.364	35.952	36.541	37.129	37.718

When the capacitances were scaled from 1pf to 25pf with an interval of 5pf using SSTL18_II_DCI, **14.858%** I/O power was being saved if we works at 1pf instead of

25pf,12.38% power is being saved if we works at 5pf instead of 25pf,9.288% I/O power was being saved if we works at 10pf instead of 25pf, 6.190% I/O power was being saved if we works at 15pf instead of 25pf,3.093% I/O power was being saved if we works at 20pf instead of 25pf.There is no change in all the other powers inspite of IO power if we do capacitive scaling from 1pf to 25pf.



4. Conclusion

Power savings were 29.885% using SSTL2_II_DCI which was maximum amongst others. This IO standard saved maximum power as compared to others when the capacitances were scaled from 1pf to25pf .Varying of capacitance has a significant change accompanied with change in IO standards. SSTL18_II had less power saving as compared to SSTL2_II_DCI. SSTL18_II saved 13.121%. of power. Using SSTL18_I a little change of 9.780522% was found in power saving. IO power varied in all the cases rest all the powers were same even though different IO standards were used. Power saving varied in IO ports. For efficient power saving accurate impedance matching IO standard has to be used at every stage which will increase the power saving. Taking different values of capacitances different power saving results can be achieved. It can be concluded that by using **SSTL2_II_DCI** IO standard out of all other SSTL based logic.
families, maximum power savings of 29.885% can be achieved.

5. Future Scope

We can also calculate the powers at Mhz and Hz of frequencies instead if 1THz which we have done in this part and can also compare the powers at low, middle and high level ranges of frequencies. Power savings can also be measured using different IO standards such as HSTL,LVCMOS,LVDCI etc.Calculations can also be done using even using 20 nm FPGA such as Artex and Kintex Some different techniques along with this technique such as frequency and voltage scalingcan be employed to have better power results.

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