International Journal of Security and Its Applications
Vol. 9, No. 6 (2015), pp. 271-278
http://dx.doi.org/10.14257/ijsia.2015.9.6.26

Thermal aware Internet of Things Enable Energy Efficient Encoder Design for Security on FPGA

Deepa Singh[1], Kanika Garg[2], Ravneet Singh[3], Bishwajeet Pandey[4], Kartik Kalia[5] and Hasmatullah Noori[6]

[1]*Department of IT, ABV-IIITM, Gwalior, India*
[2, 3, 4, 5]*Department of Computer Science, Chitkara University, Chandigarh, India*
[6]*Department of CSE, South Asian University, Delhi, India*
[1]*deepasingh.iiitm@gmail.com*, [2]*kanika.garg@chitkara.edu.in*, [3]*gyancity@gyancity.com*, [4]*kartikkalia4@gmail.com*, [5]*satshriakal555@gmail.com*, [6]*hashmatullah.noori2010@gmail.com*

Abstract

In this work, we are going to use thermal aware approach in Encoder design and also testing thermal stability by working on different ambient temperatures 298.15K, 308.15K, 318.15K, 328,15K, 338.15K and 348.15K and 358.15K. We have observe the compatibility of our device with wireless network by working on different I/O standards (LVCMOS15 and LVCMOS25) . There is 30.29% reduction in leakage power, when we scale down temperature from 358.15K to 298.15K using LVCMOS15 as I/O standard on 40nm Virtex FPGA. Leakage power is calculated for 65nm FPGA and 90nm FPGA as well .In this work, we are using Verilog Hardware Description Language.

Keywords—*Encoder, Internet of Things, FPGA, LVCMOS15, LVCMOS 25, Thermal Aware Design, Energy Efficient Design.abstract*

1. Introduction

The Internet of Things (IoT) refers to network of physical objects [1]. The internet of things is an information technology which comes third right after Internet and mobile communication network. To enable these new forms of communication, we require transceivers and IPv6 Address. IPv6 address is 128 bits long. So, we can assign 100 addresses to every atom on the surface of the earth. Therefore, we have plenty of IPv6 address, which we can assign for every Encoder [2] and make it Internet of Things (IoTs) enable Encoder as shown in Figure 1. Each object has a feature of an IP address for internet connectivity. Finally, communication takes place between these objects and other Internet-enabled devices [3]. Energy conservation and security are major concern in Internet of Things. Figure 1 shows that internet of things is a combination of objects, network ,data and services.

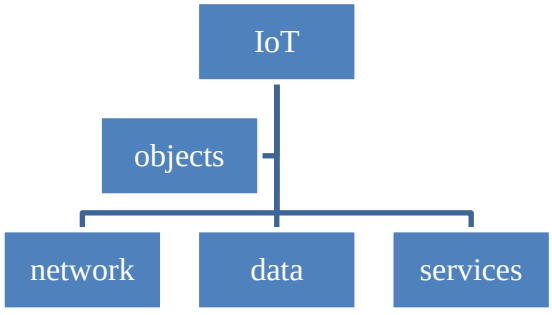


Figure 1. Short Description of Internet of Things

ISSN: 1738-9976 IJSIA

Encoders can be described as a device, circuit, system, the device that converts one form of energy, program, or algorithm that transform or translate information from one format or code to another [4]. The main function of using encoder is performance, efficiency, security or compressions. Encoders turn readable information into a different format. For example it converts a CD track into an MP3. A decoder reverses the effects of this encoding to make the file readable, for example windows media player. Another example is of a television station which compresses data into encoded format for broadcast on the digital broadcast network. Either Encoding or Decoding are done for the safe transmission of data [5]. As the security is a major concern in internet of things, the safe transmission of data and images is necessary to prevent any kind of unauthorized attacks. Energy efficient design approach is also used for Key management scheme for Body area Network. We are making energy efficient [1-6, 10] key management scheme for general purpose network using LVMCOS IO standards and three different FPGA families. We have used 16:4 bit encoder for the transmission of a private message to a recipient. The message can be encoded by using various methods, algorithms like RSA,AES,DES etc. for strong encryption so that it becomes difficult for the attacker to crack the message or data[6].

The message is encrypted as shown in the Table 1 below:

Table 1. Private Message to be Send to the Recipient

ASCII CODE	Private Message	Encoded Message
5468	Th	1
654B	eK	2
6579	ey	3
746F	to	4
756E	un	5
6C6F	lo	6
636B	ck	7
6D79	my	8
5361	Sa	9
6665	fe	10
6973	is	11
4953	43	12
3433	21	13
3231	86	14
3934	94	15

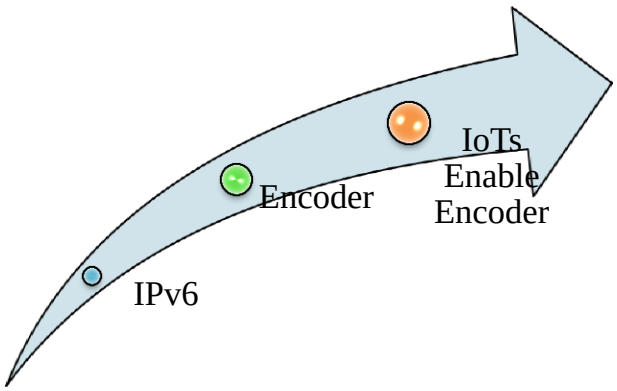
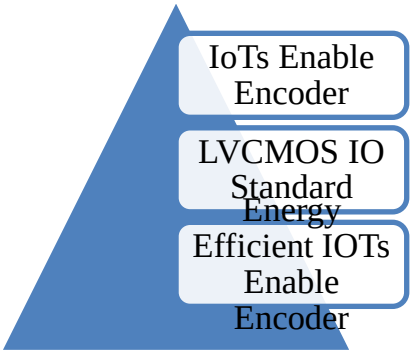


Figure 2. Internet of Things Enable Encoder

We have embedded an IP address (IPV6) in Encoder .This encoder is now network accessible. IPSec, which provides confidentiality, authentication and data integrity, is integrated in IPv6. Because of their potential to carry a virus that is designed to damage the information on computer, IPv4 ICMP packets are frequently blocked by corporate firewalls.But ICMPv6, the implementation of the Internet Control Message Protocol for IPv6, may be permitted because IPSec can be applied to the ICMPv6 packets. We test that Encoder using I/O standard (LVCMOS). LVCMOS is a low voltage (LV) class of CMOS technology integrated circuits temperatures. CMOS is complementary type of MOS. whereas, MOS is Metal Oxide Semiconductor. We are operating our IOTs Enable encoder on different 7 temperatures ranges of *298.15K-358.15K*. And, we are analyzing energy efficiency in respect of different LVCMOS IO standards used in IoTs Enable Encoder as shown in Figure 3.



Encoder Figure 3. Components of Energy Efficient IoTs Enable

As shown in Figure 4, Encoder has 16-bit data input along with 1-bit enable and 128-bit IPv6 address. It encodes 16-bit input into 4-bit output. This encoder design is a part of real encryption system. When we provide output of this encoder to any decoder, output of decoder will be similar to input of encoder. This design is also working on these principles: authentication [9], integrity, confidentiality and availability. In other words, output of encoder is encrypted text (Encoded Message) whereas input of encoder is plain text (Private Message) as per Table 1.

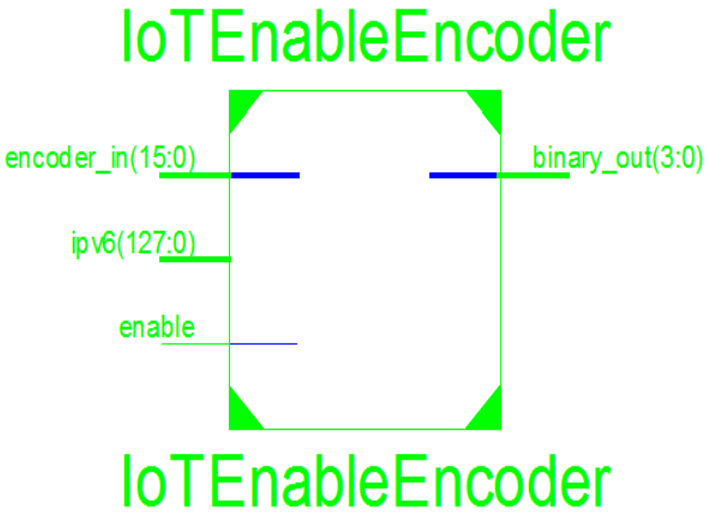


Figure 4. IoT Enable ENCODER

2. Thermal and Power Analysis

We design an IOT enable Encoder with an IP version 6 addresses (IPV6). Then we took out power readings using different temperatures on different FPGA's. FPGA is Field Programmable Gate Array. It is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence "field-programmable":

Table 2. Comparison of Power Dissipation on Different FPGA

LVCMOS15	25	35	45	55	65	75	85
40nm	1.118	1.181	1.252	1.334	1.428	1.535	1.604
65nm	0.241	0.268	0.300	0.338	0.383	0.436	0.489
90nm	0.138	0.147	0.159	0.172	0.188	0.206	0.220

When we migrate from 40nm to 65nm, and 90nm technology, then there is 78.44%, and 87.66% reduction in power dissipation on 25°C as shown in Table 2. In Table 2 also, when we migrate from 40nm to 65nm, and 90nm technology, then there is 69.51%, and 86.28% reduction in power dissipation on 85°C.

Table 3. Comparison of Power Dissipation on Different FPGA

LVCMOS25	25	35	45	55	65	75	85
40nm	1.119	1.182	1.253	1.335	1.429	1.536	1.605
65nm	0.243	0.270	0.302	0.340	0.385	0.438	0.491
90nm	0.139	0.149	0.160	0.173	0.189	0.207	0.222

When we migrate from 40nm to 65nm, and 90nm technology, then there is 77.16%, and 87.39% reduction in power dissipation on 35°C as shown in Table 3. In Table 3 also, when we migrate from 40nm to 65nm, and 90nm technology, then there is 71.48%, and 86.17% reduction in power dissipation on 75°C.

Table 4. Comparison of Power Dissipation on 40nm Virtex-6 FPGA

	25	35	45	55	65	75	85
LVCMOS15	1.118	1.181	1.252	1.334	1.428	1.535	1.604
LVCMOS25	1.119	1.182	1.253	1.335	1.429	1.536	1.605

At 40nm Virtex-6 FPGA, there is 30.29% reduction in leakage power when we scale down temperature from 358.15K to 298.15K as shown in Table 4.

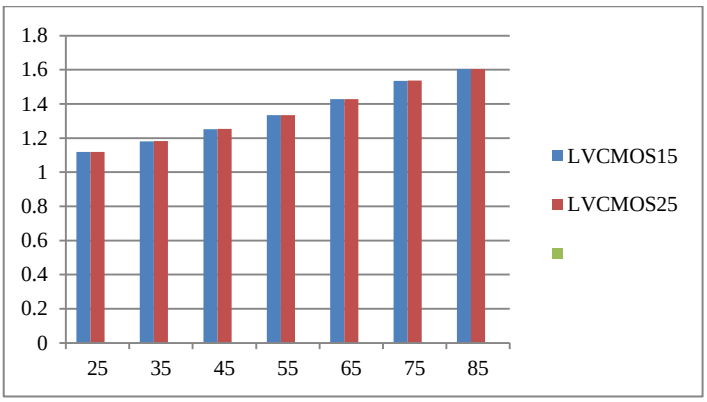


Figure 5. Leakage Power Dissipation by Different I/O Standards

Variation in IO Standard do not play significant role in change leakage power dissipation as shown in Figure 5.

Table 5. Comparison of Power Dissipation on 65nm Virtex-5 FPGA

	25	35	45	55	65	75	85
LVCMOS15	0.241	0.268	0.300	0.338	0.383	0.436	0.489
LVCMOS25	0.243	0.270	0.302	0.340	0.385	0.438	0.491

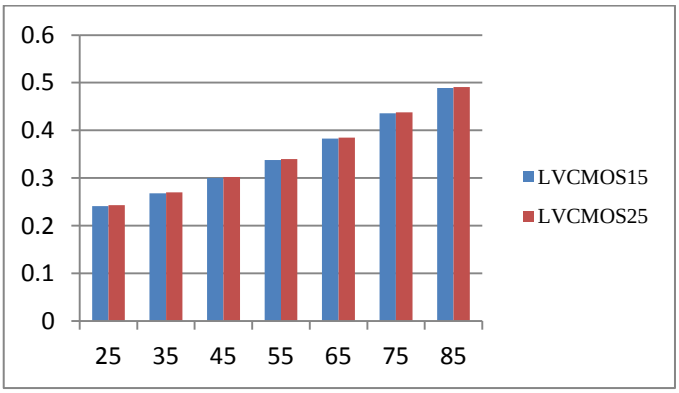


Figure 6. Leakage Power Dissipation by Different I/O Standards

At 65nm Virtex-6 FPGA, there is 50.71% reduction in leakage power when we scale down temperature from 358.15K to 298.15K as shown in Table 5. Variation in IO Standard do not play significant role in change in reduction in leakage power dissipation as shown in Figure 6 and Table 5.

Table 6. Comparison of Power Dissipation on 90nm Virtex-4 FPGA

	25	35	45	55	65	75	85
LVCMOS15	0.138	0.147	0.159	0.172	0.188	0.206	0.220
LVCMOS25	0.139	0.149	0.160	0.173	0.189	0.207	0.222

At 90nm Virtex-4 FPGA, there is 37.27% reduction in leakage power when we scale down temperature from 358.15K to 298.15K as shown in Table 6.

3. Conclusion

We observed that when we use Virtex-5 instead of Virtex -6 and Virtex-4 there is a large reduction of 50.71% when we scale down temperature from 358.15 to 298.15K using LVCMOS as an I/O standard. So we can conclude that Virtex -5 FPGA is more efficient than Virtex-4 and Virtex-6 FPGA to make energy efficient Internet of Things enable Encoder using LVCMOS I/O standard.

4. Future Scope

Like LVCMOS I/O standard we can use SSTL, GTLP, GTL, PCIX, PCI33, PCI66 and many more I/O standards for making an energy efficient Encoder. We can also use Artrix FPGA and Ultrascale Virtex instead of Virtex-4, Virtex-5, Virtex-6 as well. We can test these I/O standards on different frequencies. So there are many I/O standards and FPGA's by which we can design energy efficient Internet of Things enabled Encoder.

References

[1] K. Kaur, "Internet of Things Enabled Energy Efficient Green Communication on FPGA", IEEE 6th International Conference on Computational Intelligence and Communication Networks (CICN), Udaipur, **(2014)** November 14-16.
[2] B. Pandey, "Thermal Mechanics Based Energy Efficient FIR Filter for Digital Signal Processing", Applied Mechanics and Materials, (AMM) Journal, vol. 612, **(2014)** August, pp. 65-70.
[3] G. Verma, "Thermal and Power Aware Internet of Things Enable RAM Design on FPGA", IEEE Intl Conf on Computing for Sustainable Global Development (**INDIACOM**), Bharti Vidyapeeth, Delhi, **(2015)** March.
[4] M. Palesi, "Data encoding schemes in networks onchip", IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 30.
[5] C. P. Fan and C. H. Fang, "Efficient RC low-power bus encoding methods for crosstalk reduction", Integr, VLSI J., vol. 44, no. 1.
[6] X. Huang, "A Generic Framework for Three-Factor Authentication: Preserving Security and Privacy in Distributed Systems", IEEE Transactions on Parallel and Distributed Systems, vol. 22, no. 8.
[7] G. D. Abowd, G. R. Hayes, G. Iachello, J. A. Kientz, S. N. Patel and M. M. Stevens, "Prototypes and paratypes: Designing mobile and ubiquitous computing applications", IEEE Pervasive Computing.
[8] E. Welbourne, "Building the Internet of Things using RFID", IEEE Internet Computing, IEEE Computer Society, **(2009)** May-June.
[9] G. Kortuem, "Smart Objects as building blocks of Internet of things", IEEE Internet Computing, IEEE Computer Society, **(2010)** January-February.

Author

Kanika Garg, she completed 4 Year Bachelor of Technology in Computer Science and Engineering from Ambala College of Engineering and Applied Research (ACE&AR) in 2013. Currently, she is pursuing M.E. from Chitkara University, Punjab Campus. Her area of Interest is Internet of Things Enable Design, Energy Efficient Design, Low Power Design, High Performance Computing, Green Computing and Embedded System.

She has successfully published two research papers in "Bilingual International Conference on Information Technology: Yesterday, Today, and Tomorrow" organized by Defence Scientific Information & Documentation Centre (**DESIDOC**). DESIDOC is a subsidiary of Defence Research and Development Organisation (DRDO) under Defence Ministry of Government of India. Her paper also got acceptance in IEEE International Conference on "Computing for Sustainable Global Development" (**INDIACOM**), at Bharti Vidyapeeth in Delhi. She is Chief Scientist in Gyancity Research Lab. She has done joint research in energy efficient and thermal aware domain with Aalborg University, Denmark and Jaypee University of Information Technology, Noida. She has taken responsibility of many managerial and administrative roles in university placement and training programmes.

Bishwajeet Pandey, he is working in Centre of Excellence of Chitkara University-Punjab Campus as an Assistant professor. He has worked as Junior Research Fellow (JRF) at South Asian University (University declared under SAARC Charter) and visiting lecturer in IGNOU on weekends. He has completed M. Tech. from IIIT Gwalior and done R&D Project in CDAC-Noida. Before that, he has total 7+ year experience as Web Manager in Web Sanchar India, Assistant Professor at Fortune Bright Paramedical.

Institute, ASP.NET 2.0 Developer at Tours Lovers Private Ltd and IT Manager at La Care Farma Ltd. He has received Gate Fellowship from Ministry of Human Resource and Development, Government of India and Junior Research Fellowship from UGC.He is a Life Member of Computer Society of India (CSI) and Professional Member of IEEE. He is working with more than 80 Co-Researcher from Industry and Academia to create a globally educational excellence in Gyancity Research Lab and Chitkara University Research and Innovation Network (CURIN). He has authored and coauthored over 125 papers in SCI/SCOPUS/Peer Reviewed Journals and IEEE/Springer Conference proceedings in areas of Low Power Research in VLSI Design, Green Computing, and Electronic Design Automation. He has published paper in conferences in IIT, NIT, DRDO in India and Vietnam, Indonesia, Sri Lanka, Singapore, Pakistan, Hong Kong, Korea and Russia and so on. He has filled 2 patents in Patent Office in Intellectual Property Building Delhi and also authored 2 books available for sale on Amazon and Flipkart. He got best paper award in conferences in ICAMEM-2014 Hong Kong, CICN-2014 Udaipur, ICNCS-2013 Singapore, and ICCCV-2013 Coimbatore. He is a technical programme committee (TPC) member in various conferences across globe.