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Low Voltage Complementary Metal Oxide Semiconductor Based Internet of Things Enable Energy Efficient RAM Design on 40nm and 65nm FPGA

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Abstract

In this work, we are making Energy Efficient Internet of Things (IoTs) Enable RAM. In order to make it energy efficient, we are using low voltage complementary metal oxide semiconductor (LVCMOS) Standards. We are using the 3 different members of LVCMOS IO standards family at different FGPA (virtex-5 and virtex-6) and searching the most energy efficient among them. We are inserting 128-bit IP address in RAM to make internet of things enable RAM. Finally, we are operating our IOTs Enable RAM with different operating frequency of I3, I5, I7, Moto-E and Moto-X.

Keywords*: RAM, Internet of Things, FPGA, LVDCI Thermal Aware Design, Energy Efficient Design*

1. Introduction

The internet of things refers to wireless network between objects, usually the network will be wireless and self configuring such as household appliances or any object[1,8]. It ensures any place connectivity for anyone and for anything. It ensures better relationship between human and nature. In the IoT, things are expected to actively participate in business and information where they are enabled to interact and communicate among themselves and with the environment by exchanging data and information they get from the environment [2]. Internet of Things (IoT) consists of several tiny devices connected together to form a collaborative computing environment. IoT imposes peculiar constraints in terms of connectivity, computational power and energy budget. An example of IoT can be: a lot of aged people live alone in their homes. There is no one to help them if any emergency arrives. So if there are wireless sensors throughout their houses then all their activity levels, sleeping levels can be measured easily. Alerts and notifications are automatically sent to the health care services and authorized family members if something abnormal happens with them .To achieve IoT we need a universal protocol to combine several heterogeneous devices. This protocol should be: simple, lightweight, loosely-coupled, scalable, flexible and standard [5, 6].

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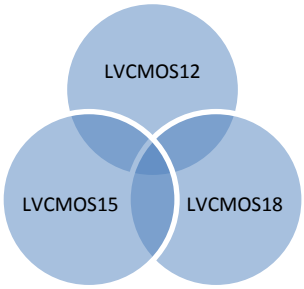

Figure 1. Different LVCMOS IO Standards

LVCMOS is an acronym for low voltage complementary metal oxide semiconductor [9, 10]. LVCMOS is the most energy efficient one because it is low voltage version of CMOS logic family, which is well-known for its low power dissipation [4, 7]. Depending on the output driver supply voltage (Vcco), there are five types of LVCMOS I/O standard. The Vcco of LVCMOS12, LVCMOS15, LVCMOS18 is 1.2V, 1.5V, 1.8V and.

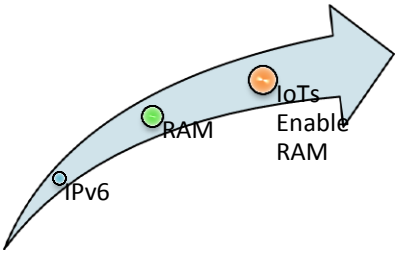

Figure 2. Internet of Things Enable RAM

We have enabled RAM with an IP address IPV6. We have measured I/O power dissipation and leakage power dissipation on different processor frequencies namely (I3, I5, I7, and Motorola) as shown in Table 1.

Table 1. Operating Frequency of Different Processor

Processor	Frequency (GHz)
I3	2.5
I5	3.6
I7	3.0
Moto-E	1.2
Moto-X	1.7

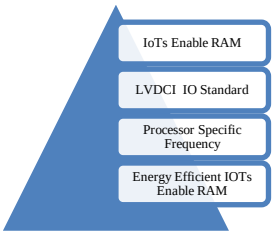

Figure 3. Components of Energy Efficient IoTs Enable RAM

As shown in Figure 4, RAM has 32-bit data input along with 16-bit write address and 16-bit read address. In case of read operation, the data stored in RAM at particular location defined by read address will go to data output port. In case of write operation, the data receive at input port will store in RAM at particular location defined by write address.

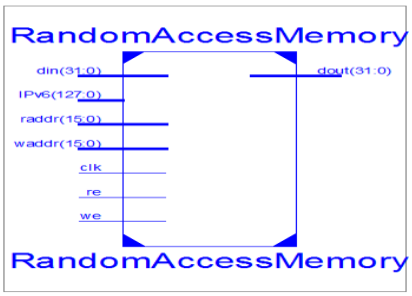

Figure 4. IoTs Enable RAM

2. Thermal and Power Analysis

We design an IOT enable RAM with an IP version 6 addresses (IPV6). Then we took out power readings using different LVCMOS Standards.

Table 2. Clock Power on 65nm and 40nm FPGA for LVCMOS12

	65nm Virtex-5	40nm Virtex-6
1.2GHz	0.061	0.057
1.7GHz	0.094	0.083
2.5GHz	0.237	0.122
3.0GHz	0.417	0.146
3.6GHz	0.762	0.176

On 1.2GHz operating frequency, there is 6.55% reduction in clock power when we use Virtex-6 instead of Virtex-5 as shown in Table 2 and Fig 5.

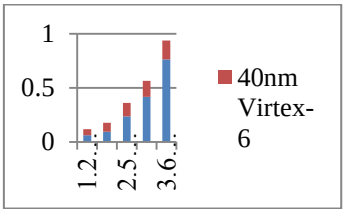

Figure 5. Clock Power on 65nm and 40nm FPGA for LVCMOS12

On 3.6 GHz operating frequency, there is 77.1 % reduction in clock power when we use Virtex-6 instead of Virtex-5 as shown in Table 2 and Fig 5.

Table 3. Signal Power on 65nm and 40nm FPGA for LVCMOS12

	65nm Virtex-5	40nm Virtex-6
1.2GHz	0.071	0.065
1.7GHz	0.101	0.092
2.5GHz	0.149	0.132
3.0GHz	0.178	0.159

3.6GHz	0.214	0.190

On 1.2GHz operating frequency, there is 8.45% reduction in Signal power when we use Virtex-6 instead of Virtex-5 as shown in Table 3 and Fig 6.

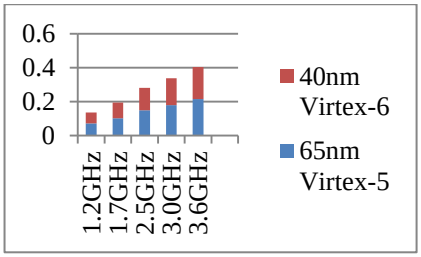

Figure 6. Signal Power on 65nm and 40nm FPGA for LVCMOS12

On 3.6 GHz operating frequency, there is 11.21% reduction in Signal power when we use Virtex-6 instead of Virtex-5 as shown in Table 3 and Fig 6.

Table 4. IO Power on 65nm and 40nm FPGA for LVCMOS12

	65nm Virtex-5	40nm Virtex-6
1.2GHz	0.008	0.018
1.7GHz	0.011	0.026
2.5GHz	0.016	0.038
3.0GHz	0.019	0.046
3.6GHz	0.023	0.055

On 1.2 GHz operating frequency, there is 55.55% reduction in I/O power when we use Virtex-5 instead of Virtex-6 as shown in Table 4 and Fig 7.

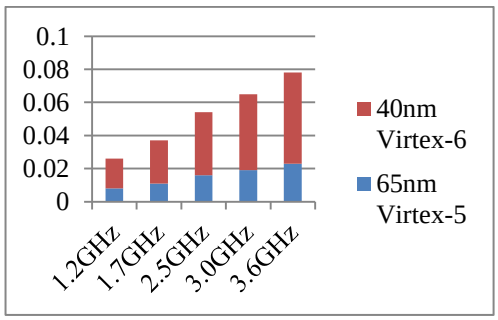

Figure 7. IO Power on 65nm and 40nm FPGA for LVCMOS12

On 3.6 GHz operating frequency, there is 32.72% reduction in I/O power when we use Virtex-5 instead of Virtex-6 as shown in Table 4 and Fig 7.

Table 5. BRAMs Power on 65nm and 40nm FPGA for LVCMOS12

	65nm Virtex-5	40nm Virtex-6
1.2GHz	2.577	2.927
1.7GHz	3.651	4.147
2.5GHz	5.370	6.098

3.0GHz	6.444	7.318
3.6GHz	7.732	8.782

On 1.2 GHz operating frequency, there is 12.19% reduction in BRAM's power when we use Virtex-5 instead of Virtex-6 as shown in Table 5 and Fig 8.

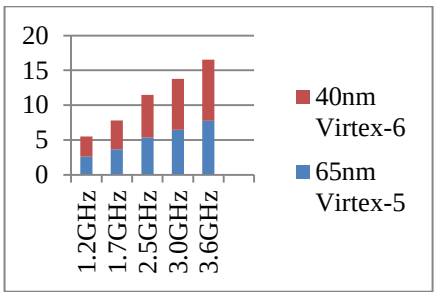

Figure 8. BRAMs Power on 65nm and 40nm FPGA for LVCMOS12

On 3.6 GHz operating frequency, there is 11.95% reduction in BRAMs power when we use Virtex-5 instead of Virtex-6 as shown in Table 5 and Fig 8.

Table 5. Leakage Power on 65nm and 40nm FPGA for LVCMOS12

	65nm Virtex-5	40nm Virtex-6
1.2GHz	0.562	0.787
1.7GHz	0.579	0.822
2.5GHz	0.610	0.881
3.0GHz	0.631	0.921
3.6GHz	0.661	0.972

On 1.2 GHz operating frequency, there is 28.5% reduction in leakage power when we use Virtex-5 instead of Virtex-6 as shown in Table 6 and Fig 9.

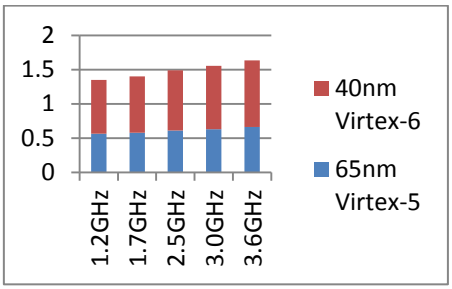

Figure 9. Leakage Power on 65nm and 40nm FPGA for LVCMOS12

On 3.6 GHz operating frequency, there is 31.99% reduction in leakage power when we use Virtex-5 instead of Virtex-6 as shown in Table 6 and Fig 9.

Table 6. Total Power on 65nm and 40nm FPGA for LVCMOS12

	65nm Virtex-5	40nm Virtex-6
1.2GHz	3.279	3.855
1.7GHz	4.437	5.171

2.5GHz	6.380	7.273
3.0GHz	7.689	8.591
3.6GHz	9.392	10.176

On 1.2 GHz operating frequency, there is 14.94% reduction in total power when we use Virtex-5 instead of Virtex-6 as shown in Table 7 and Fig 10.

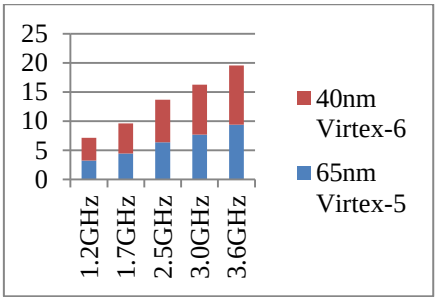

Figure 10. Total Power on 65nm and 40nm FPGA for LVCMOS12

On 3.2 GHz operating frequency, there is 7.7% reduction in total power when we use Virtex-5 instead of Virtex-6 as shown in Table 7 and Fig 10.

Table 7. Clock Power on 65nm and 40nm FPGA for LVCMOS15

	65nm Virtex-5	40nm Virtex-6
1.2GHz	0.061	0.057
1.7GHz	0.094	0.083
2.5GHz	0.237	0.122
3.0GHz	0.417	0.146
3.6GHz	0.762	0.176

On 3.6 GHz operating frequency, there is 6.5% reduction in clock power when we use Virtex-6 instead of Virtex-5 as shown in Table 8 and Fig 11.

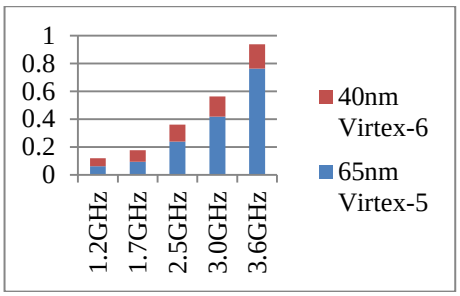

Figure 11. Clock Power on 65nm and 40nm FPGA for LVCMOS15

On 3.6 GHz operating frequency, there is 76.9% reduction in Signal power when we use Virtex-6 instead of Virtex-5 as shown in Table 8 and Fig 11.

Table 8. Signal Power on 65nm and 40nm FPGA for LVCMOS15

	65nm Virtex-5	40nm Virtex-6
1.2GHz	0.071	0.065

1.7GHz	0.101	0.092
2.5GHz	0.149	0.132
3.0GHz	0.178	0.159
3.6GHz	0.214	0.190

On 1.2 GHz operating frequency, there is 8.4% reduction in Signal power when we use Virtex-6 instead of Virtex-5 as shown in Table 9 and Fig 12.

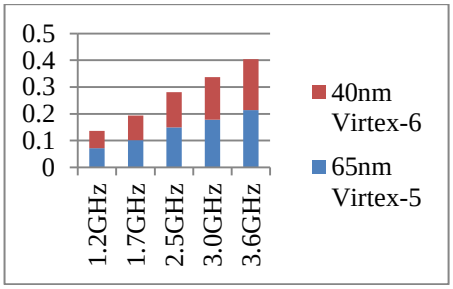

Figure 12. Signal Power on 65nm and 40nm FPGA for LVCMOS15

On 3.6 GHz operating frequency, there is 11.21% reduction in Signal power when we use Virtex-6 instead of Virtex-5 as shown in Table 9 and Fig 12.

Table 9. IO Power on 65nm and 40nm FPGA for LVCMOS15

	65nm Virtex-5	40nm Virtex-6
1.2GHz	0.008	0.018
1.7GHz	0.011	0.026
2.5GHz	0.016	0.038
3.0GHz	0.019	0.046
3.6GHz	0.023	0.055

On 1.2 GHz operating frequency, there is 55.55% reduction in I/O power when we use Virtex-5 instead of Virtex-6 as shown in Table 10 and Fig 13.

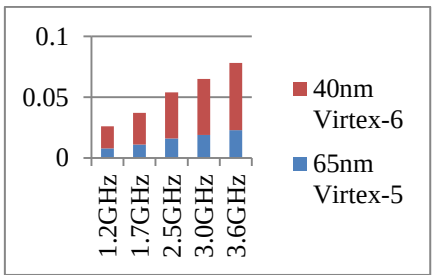

Figure 13. IO Power on 65nm and 40nm FPGA for LVCMOS15

On 3.6 GHz operating frequency, there is 32.72% reduction in I/O power when we use Virtex-5 instead of Virtex-6 as shown in Table 10 and Fig 13.

Table 10. BRAMs Power on 65nm and 40nm FPGA for LVCMOS15

	65nm Virtex-5	40nm Virtex-6
1.2GHz	2.577	2.927

1.7GHz	3.651	4.147
2.5GHz	5.370	6.098
3.0GHz	6.444	7.318
3.6GHz	7.732	8.782

On 1.2 GHz operating frequency, there is 11.95% reduction in BRAM's power when we use Virtex-5 instead of Virtex-6 as shown in Table 11 and Fig 14.

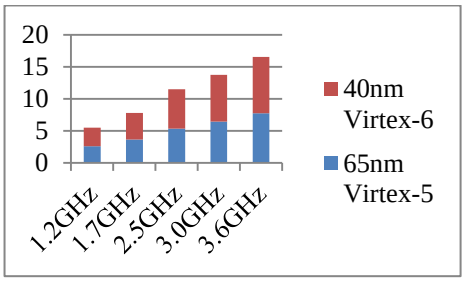

Figure 14. BRAMs Power on 65nm and 40nm FPGA for LVCMOS15

On 3.6 GHz operating frequency, there is 11.95% reduction in BRAM's power when we use Virtex-5 instead of Virtex-6 as shown in Table 11 and Fig 14.

Table 11. Leakage Power on 65nm and 40nm FPGA for LVCMOS15

	65nm Virtex-5	40nm Virtex-6
1.2GHz	0.563	0.787
1.7GHz	0.580	0.822
2.5GHz	0.610	0.882
3.0GHz	0.632	0.921
3.6GHz	0.661	0.972

On 1.2 GHz operating frequency, there is 28.4% reduction in leakage power when we use Virtex-5 instead of Virtex-6 as shown in Table 12 and Fig 15.

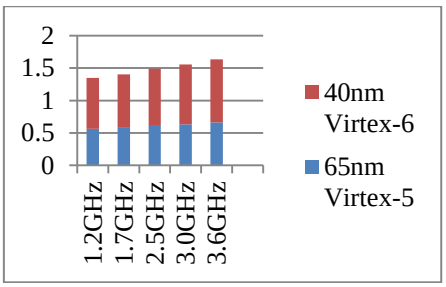

Figure 15. Leakage Power on 65nm and 40nm FPGA for LVCMOS15

On 3.6 GHz operating frequency, there is 31.99% reduction in leakage power when we use Virtex-5 instead of Virtex-6 as shown in Table 12 and Fig 15.

Table 12. Total Power on 65nm and 40nm FPGA for LVCMOS15

	65nm Virtex-5	40nm Virtex-6
1.2GHz	3.280	3.856
1.7GHz	4.437	5.171
2.5GHz	6.381	7.273
3.0GHz	7.689	8.592
3.6GHz	9.392	10.176

On 1.2 GHz operating frequency, there is 14.9% reduction in total power when we use Virtex-5 instead of Virtex-6 as shown in Table 13 and Fig 16.

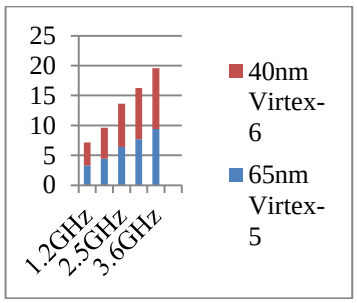

Figure 16. Total Power on 65nm and 40nm FPGA for LVCMOS15

On 3.6 operating frequency, there is 7.7% reduction in Tootle power when we use Virtex-5 instead of Virtex-6 as shown in Table 13 and Fig 16.

Table 13. Clock Power on 65nm and 40nm FPGA for LVCMOS18

	65nm Virtex-5	40nm Virtex-6
1.2GHz	0.061	0.057
1.7GHz	0.094	0.083
2.5GHz	0.237	0.122
3.0GHz	0.417	0.146
3.6GHz	0.762	0.176

On 1.2 operating frequency, there is 6.5 % reduction in clock power when we use Virtex-6 instead of Virtex-5 as shown in Table 14 and Fig 17.

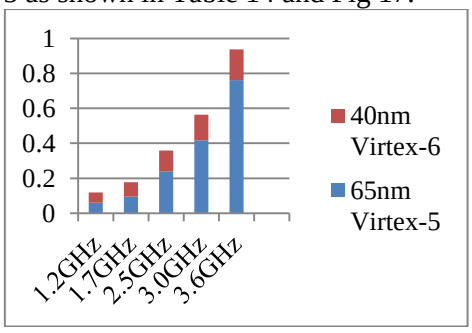

Figure 17. Clock Power on 65nm and 40nm FPGA for LVCMOS18

On 3.6 operating frequency, there is 76.9 % reduction in clock power when we use Virtex-6 instead of Virtex-5 as shown in Table 14 and Fig 17.

Table 14. Signal Power on 65nm and 40nm FPGA for LVCMOS18

	65nm Virtex-5	40nm Virtex-6
1.2GHz	0.071	0.065
1.7GHz	0.101	0.092
2.5GHz	0.149	0.132
3.0GHz	0.178	0.159
3.6GHz	0.214	0.190

On 1.2 operating frequency, there is 8.4 % reduction in Signal power when we use Virtex-6 instead of Virtex-5 as shown in Table 15 and Fig 18.

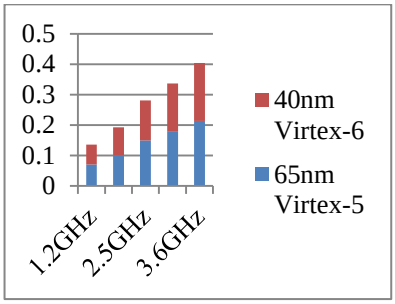

Figure 18. Signal Power on 65nm and 40nm FPGA for LVCMOS18

On 1.2 operating frequency, there is 8.4 % reduction in Signal power when we use Virtex-6 instead of Virtex-5 as shown in Table 15 and Fig 18.

Table 15. IO Power on 65nm and 40nm FPGA for LVCMOS18

	65nm Virtex-5	40nm Virtex-6
1.2GHz	0.008	0.018
1.7GHz	0.011	0.026
2.5GHz	0.016	0.038
3.0GHz	0.019	0.046
3.6GHz	0.023	0.055

On 1.2 operating frequency, there is 55.5 % reduction in I/O power when we use Virtex-6 instead of Virtex-5 as shown in Table 16 and Fig 19.

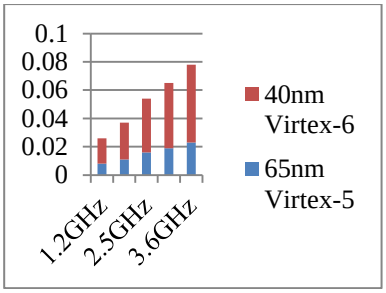

Figure 19. IO Power on 65nm and 40nm FPGA for LVCMOS18

On 3.6 operating frequency, there is 58.18 % reduction in I/O power when we use Virtex-6 instead of Virtex-5 as shown in Table 16 and Fig 19.

Table 16. BRAMs Power on 65nm and 40nm FPGA for LVCMOS18

	65nm Virtex-5	40nm Virtex-6
1.2GHz	2.577	2.927
1.7GHz	3.651	4.147
2.5GHz	5.370	6.098
3.0GHz	6.444	7.318
3.6GHz	7.732	8.182

On 1.2 operating frequency, there is 11.95 % reduction in BRAM's power when we use Virtex-5 instead of Virtex-6 as shown in Table 17 and Fig 20.

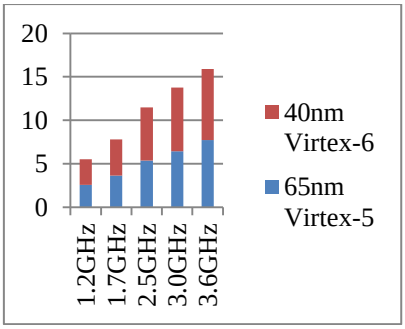

Figure 20. BRAMs Power on 65nm and 40nm FPGA for LVCMOS18

On 3.6 operating frequency, there is 5.4% reduction in BRAM's power when we use Virtex-5 instead of Virtex-6 as shown in Table 17 and Fig 20.

Table 17. Leakage Power on 65nm and 40nm FPGA for LVCMOS18

	65nm Virtex-5	40nm Virtex-6
1.2GHz	0.563	0.788
1.7GHz	0.580	0.822
2.5GHz	0.611	0.882
3.0GHz	0.632	0.922
3.6GHz	0.662	0.972

On 1.2 operating frequency, there is 28.55 % reduction in Leakage power when we use Virtex-5 instead of Virtex-6 as shown in Table 18 and Fig 21.

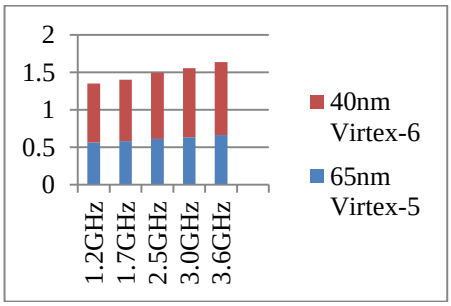

Figure 21. Leakage Power on 65nm and 40nm FPGA for LVCMOS18

On 3.6 operating frequency, there is 31.8 % reduction in Leakage power when we use Virtex-5 instead of Virtex-6 as shown in Table 18 and Fig 21.

Table 18. Total Power on 65nm and 40nm FPGA for LVCMOS18

	65nm Virtex-5	40nm Virtex-6
1.2GHz	3.281	3.856
1.7GHz	4.438	5.172
2.5GHz	6.382	7.274
3.0GHz	7.690	8.592
3.6GHz	9.393	10.176

On 1.2 operating frequency, there is 14.93 % reduction in Total power when we use Virtex-6 instead of Virtex-5 as shown in Table 19 and Fig 22.

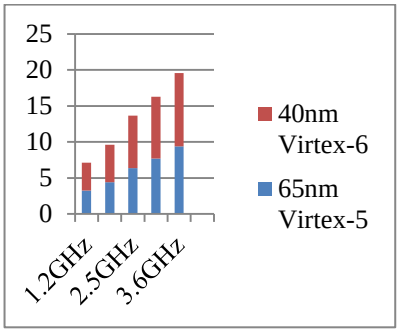

Figure 22. Total Power on 65nm and 40nm FPGA for LVCMOS18

On 3.6 operating frequency, there is 7.6 % reduction in Total power when we use Virtex-6 instead of Virtex-5 as shown in Table 19 and Fig 22.

3. Conclusion

We observed that on 3.6 operating frequency, there is 7.6 % reduction in Total power when we use Virtex-6 instead of Virtex-5 in Total power dissipation. So we can conclude that Virtex-5 is least efficient and Virtex-5 is most efficient FPGA when we use LVCMOS as an I/O standard.

4. Future Scope

Like LVCMOS_15 & LVMOS_18 standards we can use HSTL, GTLP, GTL, PCIX, PCI33, PCI66 and many more I/O standards for making an energy efficient RAM. We can use FPGA Virtex- 4, instead of Virtex-5, Virtex- 6 as well. We can test these I/O standards on different frequencies .So there are many I/O standards and FPGA's by which we can design energy efficient Internet of Things enabled RAM.

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