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IO Standards based Energy Efficient Room Temperature Sensor Design

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Abstract

In this work energy efficient room temperature sensor is designed using various IO standards. This design is implemented on Kintex-7 FPGA, XC7K70T device and FBG676 package. The simulator used is Xilinx 14.6 and Verilog is used as the verification language. The power analysis is done using XPower estimator. The various IO standards implemented in the design are HSUL_12, Mobile_DDR, PCI33_3 and SSTL18_II. The temperature scaling is being done for analyzing the behavior of circuit at different temperature values. The temperature is scaled from 50^{o}C to 45^{o}C, 40^{o}C, 35^{o}C, 30^{o}C and 25^{o}C. There is reduction of 17.39%, 65.22% and 91.30% in IO power when we migrate our design from SSTL18_II to HSUL_12, Mobile_DDR and PCI33_3 IO standards respectively. The maximum reduction in total power is achieved when the design is migrated from SSTL18_II to PCI33_3 IO standard. The reduction in total power is 26.32%, 24.69%, 22.72%, 20.83%, 18.87% and 16.95% at 25^{o}C, 30^{o}C, 35^{o}C, 40^{o}C, 45^{o}C and 50^{o}C respectively when the IO standard is migrated from SSTL18_II to PCI33_3.

Keywords: *Energy efficient, HSUL_12, Mobile_DDR, PCI33_3, Room Temperature Sensor, SSTL18_II, Temperature scaling*

1. Introduction

The room temperature sensor senses the temperature of room. It has various input signals: clock, room temperature, room temperature threshold 1 and 2, additional airflow. The output is in the form of ring fire alarm and no fire. The top level schematic of room temperature sensor is shown in Figure 1.

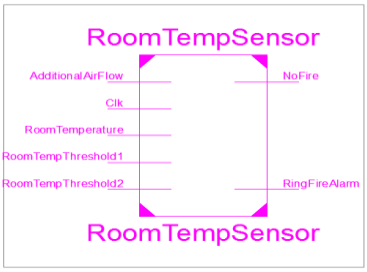

Figure 1. Top Level Schematic of Room Temperature Sensor

HSUL_12 is High Speed Unterminated Logic. This standard is for LPDDR2 and LPDDR3 memory buses. It requires a differential amplifier input buffer and a push-pull output buffer. This standard is supported by ultras scale devices for single ended signaling

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and differential signaling [1]. Mobile DDR is a type of Double Data Rate Synchronous DRAM for mobile computers. It is also known as mDDR, Low Power DDR, or LPDDR [2]. PCI is Peripheral Component Interconnect. It is a standard that describes how the peripheral components of a system can be connected together in a structured and controlled manner [3]. The Stub-Series Terminated Logic (SSTL) for 2.5V (SSTL2) and 1.8V (SSTL18) standards are for general purpose memory buses. The SSTL2 standard has two classes; Class I is for unidirectional and class II is for bidirectional signaling. Virtex-6 FPGA I/O supports both standards for single-ended signaling and differential signaling. This standard requires a differential amplifier input buffer and a push-pull output buffer [4]. The Figure 2 shows the various IO standards used in the design. The Figure 3 shows the temperature scaling from 25°C to 50°C.

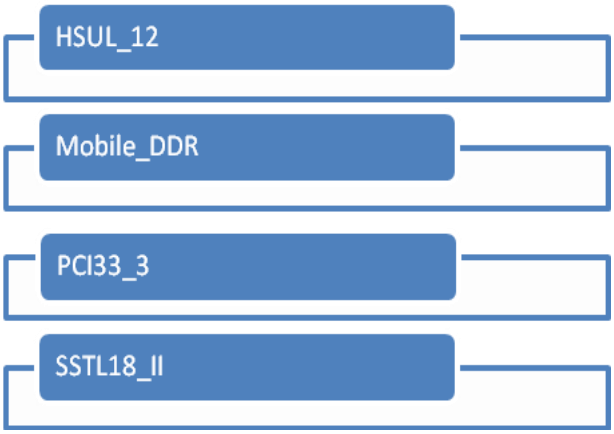

Figure 2. IO Standards Used In Design

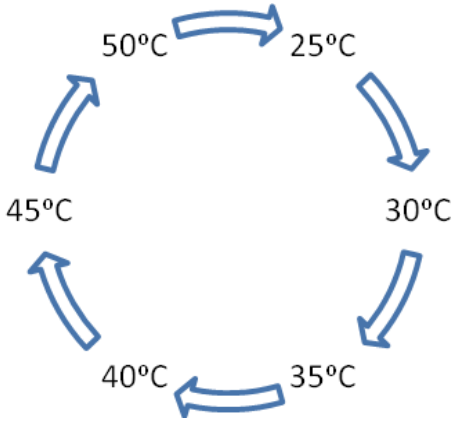

Figure 3. Temperature Scaling Process

2. Literature Review

In the energy efficient design of ALU, when LVCMOS is replaced with Mobile_DDR, there is 69.07% reduction in IO power and 29.36% leakage power reduction [5]. When green image ALU is designed using SSTL IO standards, there is IO power reduction of 45.55% and clock power reduction of 20.50% when SSTL18_I_DCI is used as compared to SSTL18_II IO Standard [6]. In energy efficient design of vedic multiplier, there is leakage power reduction of 94.64% 61.57% with LVCMOS18 IO standard when the design is migrated from Virtex-5 to Virtex-6 and Virtex-4 [7].

3. Results

3.1. Power Dissipation for PCI33_3 IO standard

Table 1. Power Dissipation for PCI33_3 IO standard

Power	25°C	30°C	35°C	40°C	45°C	50°C
Clocks	0.007	0.007	0.007	0.007	0.007	0.007
Logic	0.000	0.000	0.000	0.000	0.000	0.000
Signals	0.000	0.000	0.000	0.000	0.000	0.000
IOs	0.002	0.002	0.002	0.002	0.002	0.002
Leakage	0.047	0.052	0.059	0.067	0.077	0.089
Total	0.056	0.061	0.068	0.076	0.086	0.098

According to Table 1, when PCI33_3 is used for designing the room temperature sensor, there is a reduction of 13.48%, 24.72%, 33.71%, 41.57% and 47.19% in leakage power when we scale down the temperature from 50°C to 45°C, 40°C, 35°C, 30°C and 25°C respectively.

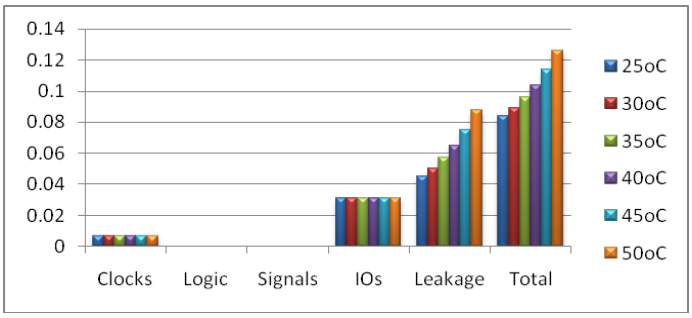

Figure 4. Power Dissipation for PCI33_3 IO Standard

The total power reduction is 12.24%, 22.45%, 30.61%, 37.76% and 42.86% as we scale down the temperature 50°C to 45°C, 40°C, 35°C, 30°C and 25°C respectively. The clock power and IO power remains the same for all the temperature values. There is no logic power and signal power for the circuit as shown in Figure 4.

3.2. Power Dissipation for Mobile_DDR IO standard

Table 2. Power Dissipation for Mobile_DDR IO Standard

Power	25°C	30°C	35°C	40°C	45°C	50°C
Clocks	0.007	0.007	0.007	0.007	0.007	0.007
Logic	0.000	0.000	0.000	0.000	0.000	0.000
Signals	0.000	0.000	0.000	0.000	0.000	0.000
IOs	0.008	0.008	0.008	0.008	0.008	0.008
Leakage	0.045	0.050	0.057	0.065	0.075	0.088
Total	0.060	0.065	0.072	0.080	0.090	0.103

According to Table 2, in the design of room temperature sensor using Mobile_DDR IO standard, there is leakage power reduction of 14.77%, 26.14%, 35.23%, 43.18% and 48.86% when we scale down the temperature from 50°C to 45°C, 40°C, 35°C, 30°C and 25°C respectively. There is total power reduction of 12.62%, 22.33%, 30.09%, 36.89% and 41.75% as the temperature is scaled down from 50°C to 45°C, 40°C, 35°C, 30°C and 25°C respectively. The clock power and IO power remains the same for all the temperature values. The logic power and signal power is zero as shown in Figure 5.

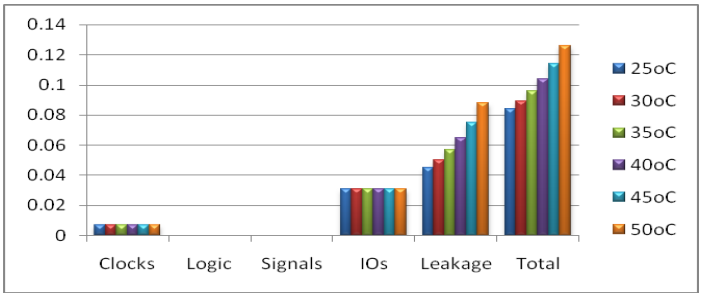

Figure 5. Power Dissipation for Mobile_DDR IO Standard

3.3. Power Dissipation for HSUL_12 IO Standard

Table 3. Power Dissipation for HSUL_12 IO Standard

Power	25°C	30°C	35°C	40°C	45°C	50°C
Clocks	0.007	0.007	0.007	0.007	0.007	0.007
Logic	0.000	0.000	0.000	0.000	0.000	0.000
Signals	0.000	0.000	0.000	0.000	0.000	0.000
IOs	0.019	0.019	0.019	0.019	0.019	0.019
Leakage	0.045	0.050	0.056	0.065	0.075	0.087
Total	0.071	0.076	0.083	0.091	0.101	0.113

As per Table 3, in case of the room temperature sensor design using HSUL_12 IO standard, the leakage power reduction is 13.79%, 25.29%, 35.63%, 42.53% and 48.28% when we scale down the temperature from 50°C to 45°C, 40°C, 35°C, 30°C and 25°C respectively. The total power reduction is 10.62%, 19.47%, 26.55%, 32.74% and 37.17% as the temperature is scaled down from 50°C to 45°C, 40°C, 35°C, 30°C and 25°C respectively. The logic power and signal power is zero. The clock power and IO power remains the same for all temperature values as shown in Figure 6.

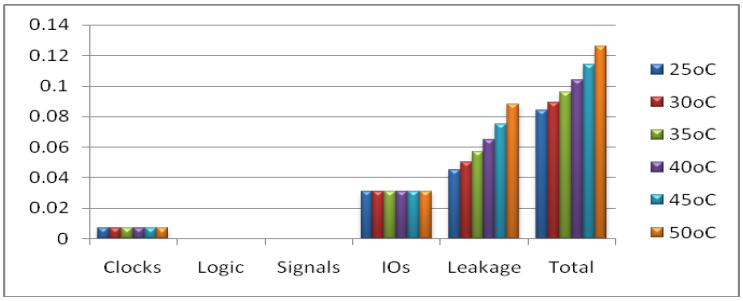

Figure 6. Power Dissipation for HSUL_12 IO Standard

3.4. Power Dissipation for SSTL18_II IO Standard

Table 4. Power Dissipation for SSTL18_II IO Standard

Power	25°C	30°C	35°C	40°C	45°C	50°C
Clocks	0.007	0.007	0.007	0.007	0.007	0.007
Logic	0.000	0.000	0.000	0.000	0.000	0.000
Signals	0.000	0.000	0.000	0.000	0.000	0.000
IOs	0.023	0.023	0.023	0.023	0.023	0.023
Leakage	0.045	0.050	0.057	0.065	0.075	0.088
Total	0.076	0.081	0.088	0.096	0.106	0.118

According to Table 4, when SSTL18_II is used for designing the room temperature sensor, there is a reduction of 14.77%, 26.14%, 35.23%, 43.18% and 48.86% in leakage power when we scale down the temperature from 50°C to 45°C, 40°C, 35°C, 30°C and 25°C respectively. The total power reduction is 10.17%, 18.64%, 21.55%, 31.36% and 35.59% as we scale down the temperature 50°C to 45°C, 40°C, 35°C, 30°C and 25°C respectively. The clock power and IO power remains the same for all the temperature values. There is no logic power and signal power for the circuit as shown in Figure 7.

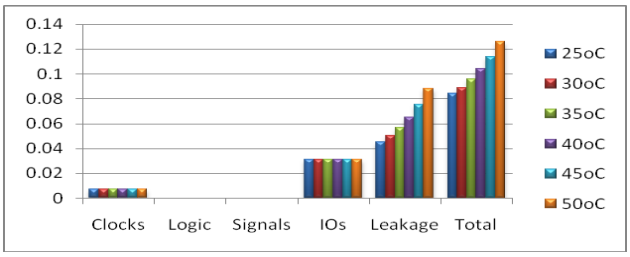

Figure 7. Power Dissipation for SSTL18_II IO Standard

4. Power Analysis

4.1. IO Power Dissipation at Different Temperature Values

Table 5. IO Power Dissipation at Different Temperature Values

Temperature	PCI33_3	Mobile_DDR	HSUL_12	SSTL18_II
25 °C- 50 °C	0.002	0.008	0.019	0.023

According to Table 5, for designing the room temperature sensor at different temperature values (25 °C- 50 °C), there is IO power reduction of 17.39%, 65.22% and 91.30% when the IO standard is migrated from SSTL18_II, to HSUL_12, Mobile_DDR and PCI33_3 respectively. The variations in IO power is shown in Figure 8.

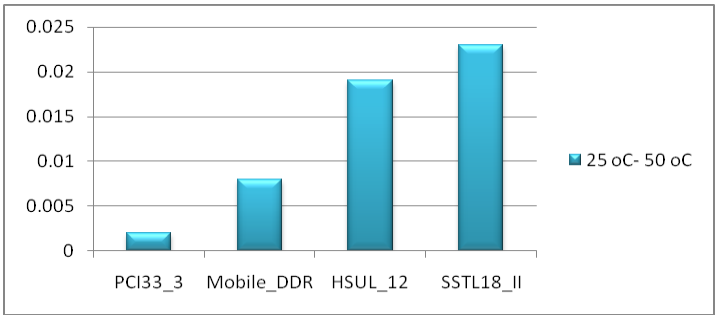

Figure 8. IO Power Dissipation at Different Temperature Values

4.2. Leakage Power Dissipation at Different Temperature Values

Table 6. Leakage Power Dissipation at Different Temperature Values

Temperature	PCI33_3	Mobile_DDR	HSUL_12	SSTL18_II
25 °C	0.047	0.045	0.045	0.045
30 °C	0.052	0.050	0.050	0.050
35 °C	0.059	0.057	0.056	0.057
40 °C	0.067	0.065	0.065	0.065
45 °C	0.077	0.075	0.075	0.075
50 °C	0.089	0.088	0.087	0.088

According to Table 6, for the design of room temperature sensor at 25°C temperature, there is leakage power reduciton of 4.26% when we migrate from PCI33_3 IO standard to other IO standards. For 30°C temperature, the leakage power reduction is 3.85% as the IO standard is migrated from PCI33_3 to other IO standards. For 35°C temperature, there is a reduction of 3.39% when we migrate from PCI33_3 to Mobile_DDR, SSTL IO standards and the reduction is 5.08% when we migrate from PCI33_3 to HSUL_12 IO standard.

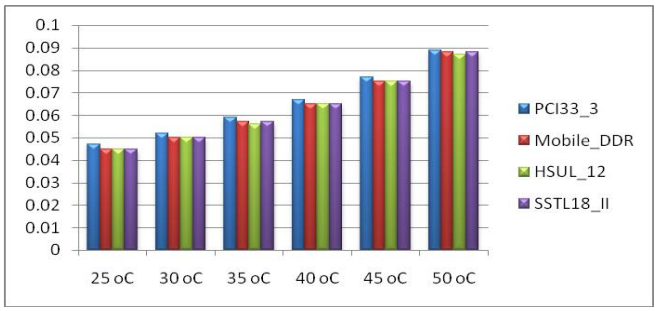

Figure 9. Leakage Power Dissipation at Different Temperature Values

For 40°C, the leakage power reduction is 2.99% when we migrate from PCI33_3 to other IO standards. For 45°C, the leakage power reduction is 2.59% when we migrate from PCI33_3 to other IO standards. For 50°C, the leakage power reduction is 2.25% when we migrate from PCI33_3 to HSUL_12 IO standard. The Figure 9 shows the variation in Leakage power for various IO standards at different temperature values.

4.3. Total Power Dissipation at Different Temperature Values

Table 7. Total Power Dissipation at Different Temperature Values

Temperature	PCI33_3	Mobile_DDR	HSUL_12	SSTL18_II
25 °C	0.056	0.060	0.071	0.076
30 °C	0.061	0.065	0.076	0.081
35 °C	0.068	0.072	0.083	0.088
40 °C	0.076	0.080	0.091	0.096
45 °C	0.086	0.090	0.101	0.106
50 °C	0.098	0.103	0.113	0.118

According to Table 7, for the design of room temperature sensor at 25°C temperature, there is total power reduction of 6.57%, 21.05%, 26.32% when we migrate from SSTL18_II to HSUL_12, Mobile_DDR and PCI33_3 respectively. For 30°C temperature, the total power reduction is 6.17%, 19.75%, 24.69% as the IO standard is migrated from SSTL18_II to HSUL_12, Mobile_DDR and PCI33_3 respectively. For 35°C temperature, the total power reduction is 5.68%, 18.88%, 22.72% as the IO standard is migrated from SSTL18_II to HSUL_12, Mobile_DDR and PCI33_3 respectively.

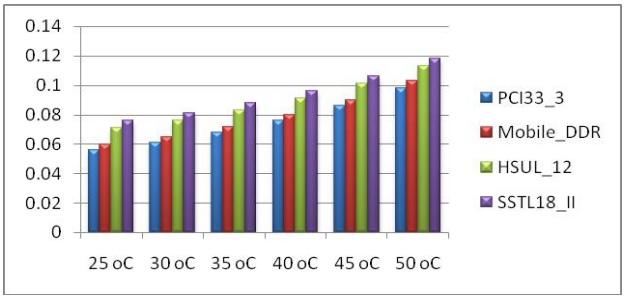

Figure 10. Total Power Dissipation at Different Temperature Values

For 40°C temperature, the total power reduction is 5.21%, 16.67%, 20.83% as we migrate the IO standard from SSTL18_II to HSUL_12, Mobile_DDR and PCI33_3 respectively. For 45°C temperature, the total power reduction is 4.72%, 15.09%, 18.87% as the IO standard is migrated from SSTL18_II to HSUL_12, Mobile_DDR and PCI33_3 respectively. For 50°C temperature, the total power reduction is 4.24%, 12.71%, 16.95% as we migrate the IO standard from SSTL18_II to HSUL_12, Mobile_DDR and PCI33_3 respectively. The variation in total power for different IO standards at different values of temperature is shown in Figure 10.

5. Conclusion

In the energy efficient design of room temperature sensor, there is reduction of 17.39%, 65.22% and 91.30% in IO power when the IO standard is migrated from SSTL18_II, to HSUL_12, Mobile_DDR and PCI33_3 respectively. There is leakage power reduction of 4.26%, 3.85%, 5.08%, 2.99%, 2.59% and 2.25% for temperature values 25 °C, 30 °C, 35 °C, 40 °C, 45 °C and 50 °C respectively when the design is migrated from PCI33_3 IO standard to other IO standards used in the implementation of design. The reduction is total power at 25 °C, 30 °C, 35 °C, 40 °C, 45 °C and 50 °C is 26.32%, 24.69%, 22.72%, 20.83%, 18.87% and 16.95% respectively when the design is migrated from SSTL18_II to PCI33_3 IO standard. This is the maximum reduction as compared to the reduction obtained with HSUL_12 and Mobile_DDR IO standards. This design is implemented using various IO standards so there is no issue of transmission line reflection. This makes our design reliable. Our design is cost effective as FPGAs are used in this design in place of fabrication and ASIC design approach.

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