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A VLSI Implementation of High Sensitive Fingerprint Sensor using Parasitic Insensitive Charge Transfer Circuit

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Abstract

This paper implements 80x64 array high sensitive fingerprint sensor with the parasitic insensitive charge transfer circuit. The fingerprint sensor cell uses an active output voltage feedback integrator. The parasitic insensitive charge transfer circuit includes a differential amplifier and two switches to remove parasitic capacitance and transfer charge. The operation is validated by HSPICE for one-pixel and RTL simulation including logic synthesis for the full chip design on condition of 0.18μm typical CMOS process and 1.8V power. The voltage difference between a ridge and valley is about 215mV after 10 clock cycles and 367mV after 20 clock cycles. The maximum frequency of cell operation is 10MHz. The layout is performed by full custom flow for one-pixel and auto P&R for the full chip. The area of the full chip is 4943μm x 3943μm and the gate count is 542,000. The area of one-pixel is 50μm x 50μm. Pitch is 50μm and image resolution is 508dpi.

Keywords: *Charge Transfer, Fingerprint Sensor, Parasitic Insensitive, Feedback Integrator, High Sensitive, RTL Synthesis*

1. Introduction

Fingerprint solution on mobile phone has been got a lot of attention recently as Apple released iPhone6s. Fingerprint sensor can benefits in both on high level of security and also user convenience [1]. Recently, fingerprint sensors are adopted on mobile application environment like a smartphone and tablet. Fingerprint data acquisition can be performed by capacitive sensing circuits [2-7]. To distinguish the capacitance produced between the finger skin and the sensor plate is the original concept of the design for a sensing circuit of the capacitive fingerprint sensors. The detecting circuit for capacitive fingerprint sensor should satisfy the requirements of low power, high sensitivity and wide output dynamic range [6]. Recent works have shown that, by applying capacitive sensing scheme, the fingerprint sensor and its readout circuit can be easily integrated in standard CMOS process. However, the main issue for capacitive sensors concerns parasitic capacitance of the sensor plate, which is formed with the interlayer under the sensor plate. The parasitic capacitance is a critical parameter in conventional sensing circuits because is larger than when a standard dielectric coating film process is used. In general, the thickness of dielectric coating film for protecting the surface of sensor is about 100 ~ 120μm. In that case, the difference of capacitance between a ridge and valley is just 0.5fF to 1fF at 50um x 50um pixel size. The value is too small for extracting an image using sensing circuit because the influence of parasitic capacitance is very critical. For low-cost production, parasitic insensitive circuit techniques should be developed.

This paper implements 80x64 array high sensitive fingerprint sensor with the parasitic insensitive charge transfer circuit. This paper adopts the fingerprint sensor circuit which uses a direct sensing method using an active output voltage feedback integrator [4]. The fingerprint sensor circuit amplifies the sensing signal by

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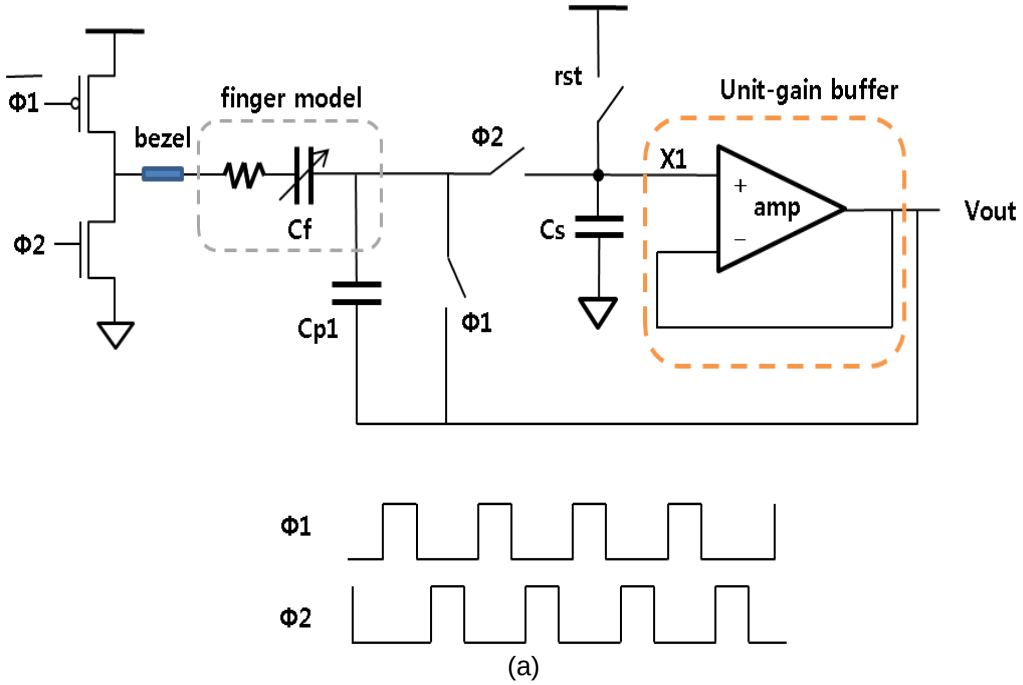
increasing integration times rather than using an amplifier or a programmable-gain-amplifier (PGA), which will improve signal-to-noise ratio (SNR) greatly and allow simple fingerprint driver architecture also. The operation is validated by HSPICE for one-pixel and RTL simulation including logic synthesis for the full chip design on condition of 0.18μm typical CMOS process and 1.8V power. The layout is performed by full custom flow for one-pixel and auto P&R for the full chip.

2. Parasitic Insensitive Charge Transfer Circuit

Capacitive sensing devices may suffer from more parasitic components in their touch sensitivity and performance. A capacitive sensor based on charge transfer circuit has also been introduced [5-7]. This paper adopts charge transfer circuit based on the active output voltage feedback integrator. Figure 1 shows the charge transfer integrator based on active output voltage feedback circuit [4]. The finger is simply modeled with a series resistor and a capacitor formed between the finger and a chip surface, Cf. A parasitic capacitor between the sensor plate and isolation metal is represented as Cp1. The sensor plate is isolated by a metal to prevent the noise from the circuit under the sensor plate as shown in figure 2, which forms a parasitic capacitance between the sensor top metal plate and under metal. Since C_{p1} is relatively large compared to C_f, it should be removed. Some methods for eliminating C_{p1} have been developed [2]. To remove simply C_{p1}, the output is applied to the bottom node of C_{p1} to maintain the same potential of the both nodes of C_{p1}, which maximizes the sensitivity of the fingerprint sensor. The fingerprint sensor using direct method uses a bezel as a contact to apply signal directly to a finger through it. A signal driven to a finger returns back through the sensor plate. $\Phi 1$ and $\Phi 2$ are the two-phase non-overlapping clocks.



(a)

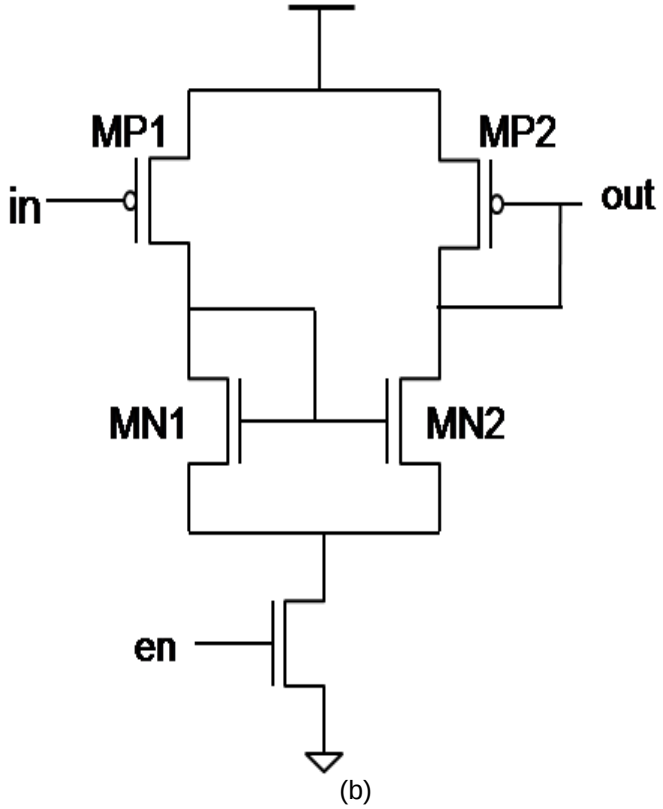


Figure 1. One Pixel Circuit of Charge Transfer based on Active Output Voltage Feedback Integrator

The clock signals, Φ 1 and Φ 2, are non-overlap control signal. When Φ 1 is on, two nodes of the parasitic capacitor, Cp1, are same potential and the influence of Cp1 is removed. Therefore, the charge of Cf only is transferred to Cs. The node of negative input of an opamp is virtually shorted to the positive input whose potential is voltage value of capacitor Cs. When Φ 2 is on, two nodes of the parasitic capacitor, Cp1, are same potential as usual because opamp operates like analog buffer. So, the influence of Cp1 is removed and Vout remains previous state. The accumulated charges in the Cf are transferred to the output capacitor, Cs. The value of Cs is 80fF and same with gate capacitance of opamp. The value of Cf changes according to ridge and valley of a finger. Figure 1(b) shows the unity-gain buffer, with the signal of en for enabling the unity-gain buffer in the evaluation phase. The role of the unity-gain buffer is tracking the voltage of the node x1. In case of 50um x 50um pixel size, the difference of Cf between a ridge and valley is about 0.5f to 1f, because the thickness of protective coating layer is more than 100μm.

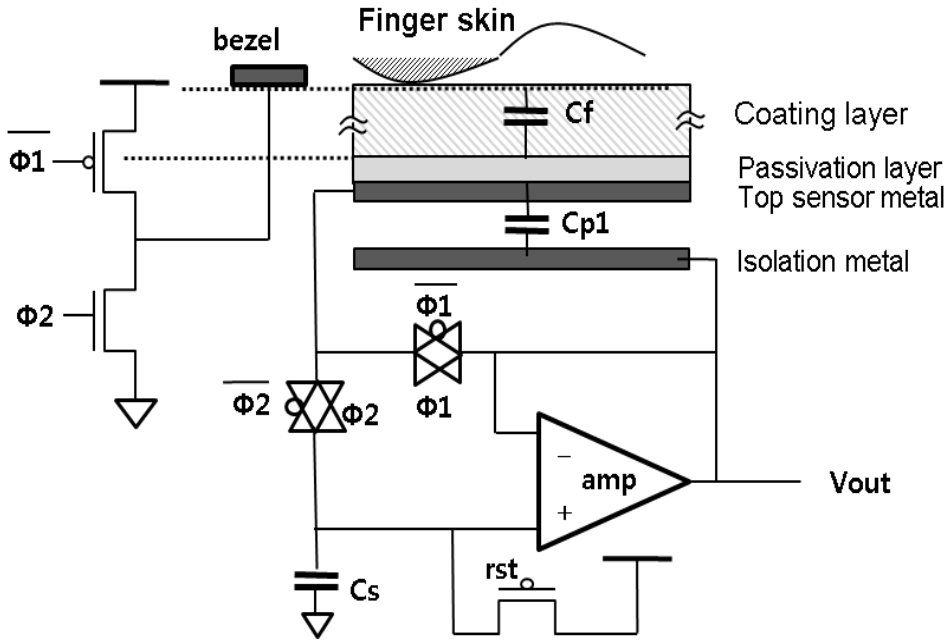


Figure 2. One Pixel CMOS Structure with Hard Coating Layer of Charge Transfer Circuit

Figure 2 shows one pixel CMOS structure with surface protective coating layer of charge transfer circuit. The capacitor formed between the sensor electrode and finger is also modeled. The sensor electrode is separated by the thin passivation layer and coating layer. Therefore, the sensor capacitor, Cf, is composed of two series-connected capacitors which are a capacitor between the electrode and passivation layer and a capacitor between coating layer and the finger skin. Because the thickness of coating layer is larger than passivation, Cf is almost same capacitor between thick coating layer and the finger skin. The parasitic capacitance of Cp1 ranges 60~100fF which is depend on sensor cell size. The signals generated from the driver are directly fed into the finger through bezel contact. To effectively remove the parasitic capacitor, the isolation metal is connected to the sensor output to maintain the same potential of both nodes of Cp1.

Figure 3 shows layout of the proposed fingerprint sensor one pixel with the active output voltage feedback integrator using 0.18 μm CMOS standard process. The area of one pixel is 50μm x 50μm and pitch is 50μm with 508dpi. To confirm the effect of proposed circuit, we extract each parasitic capacitance from the optimized layout of sensor one-pixel. Cp1 is 78fF. The difference of Cf between a ridge and valley is 0.5f to 1f at protective coating thickness of 100μm. In this paper, Cridge is 1 fF and Cvalley is 0.5fF. Functions can be seen by the HSPICE simulation of the cell with condition of 0.18μm typical parameter and 1.8V power supply after layout extraction as shown in Figure 3. Figure 4 shows the timing operation at a ridge, valley and between a ridge and valley. The voltage difference between a ridge and valley is about 215mV after 10 clock cycles and 367mV after 20 clock cycles. The maximum frequency of cell operation is 10MHz. The simulation results show the parasitic insensitive characteristics which increase touch sensitivity of the circuit.

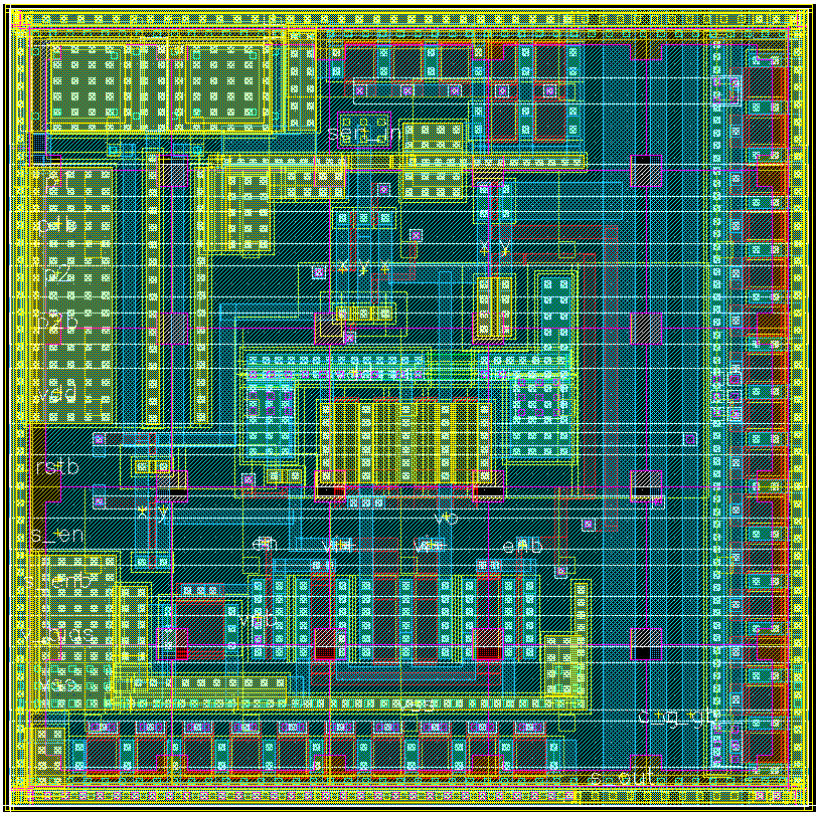


Figure 3. One Pixel Layout
(50μm x 50μm, 0.18μm CMOS Process)

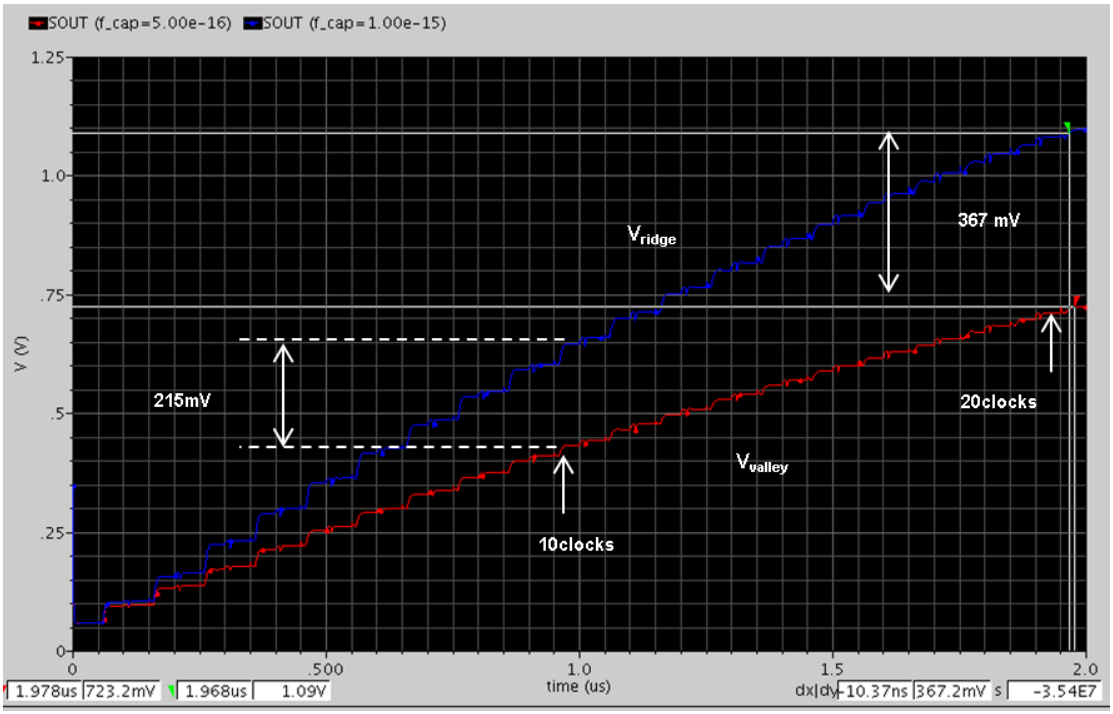


Figure 4. Timing Operation at a Ridge, Valley of One Pixel
(0.18μm CMOS Process, 1.8V Power, 10Mhz Frequency)

3. VLSI Implementation of 80x64 Pixel Array Fingerprint Sensor

Figure 5 shows the chip block diagram of the proposed area type fingerprint sensor with 80 x 64 pixel. The block of variable clock generator generates v_clk signal with variable time duration from maximum 35 clocks to minimum 5 clocks by period signal. $\Phi 1$ and $\Phi 2$ are the two-phase non-overlapping clocks. Figure 6 and 7 show the timing diagram of full chip. The signal STR_ADC means start time of ADC block and EOC means 'end of conversion' after 10 clocks of STR_ADC. Figure 8 shows the logic simulation result of digital block except analog block including sensor array. Figure 9 shows 80 x 64 pixel array chip layout and the area is 4943μm x 3943μm on 0.18μm standard CMOS process. The layout area of one pixel is 50μm x 50μm and pixel pitch is 50μm. The gate count is 542,000. The layout of 80x64 array core cell is performed by full custom design method and the full chip is performed by auto placement and routing of cell based design method.

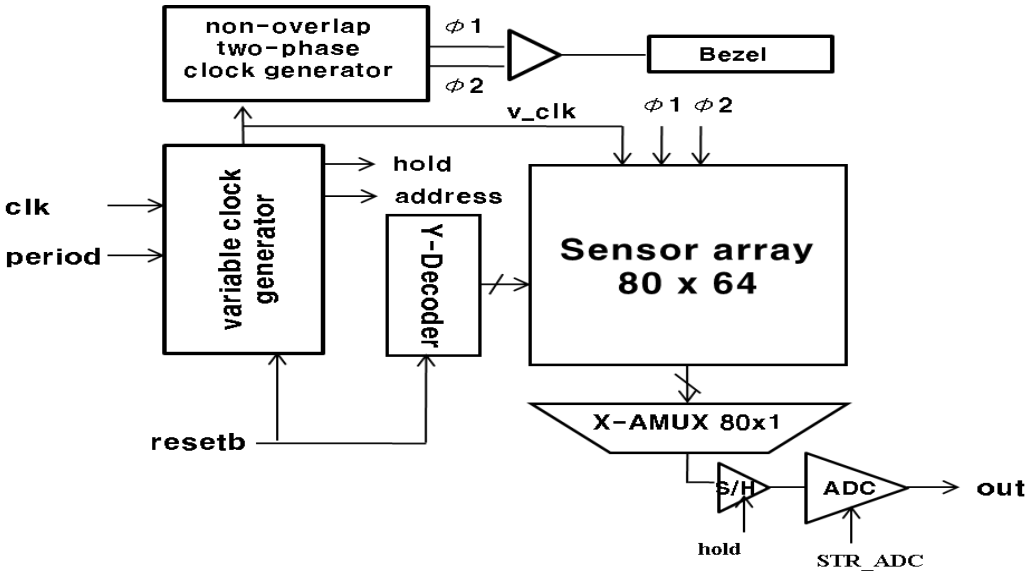


Figure 5. Chip Architecture

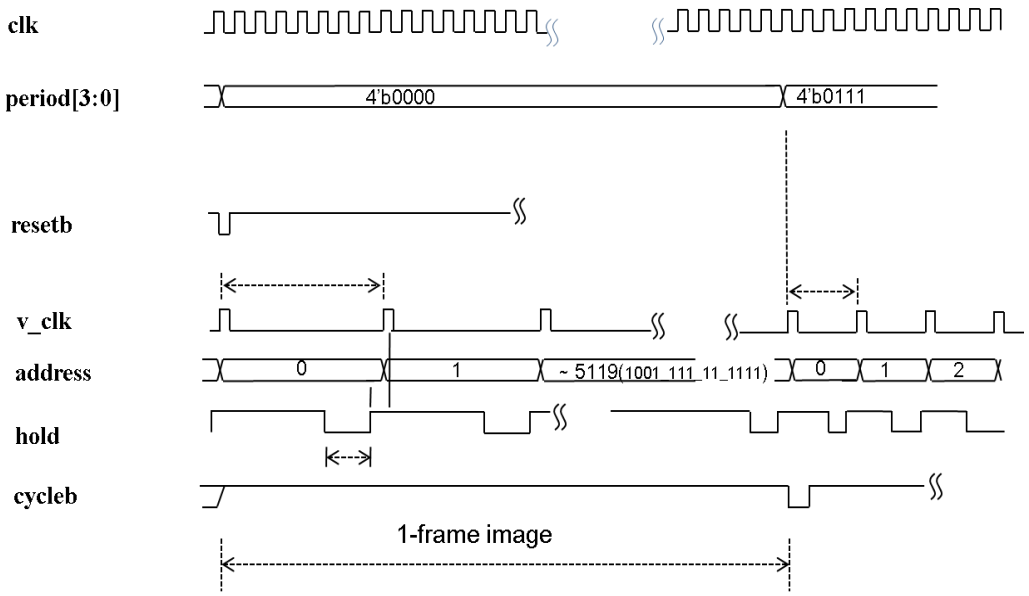


Figure 6. Timing Diagram of Fingerprint LSI

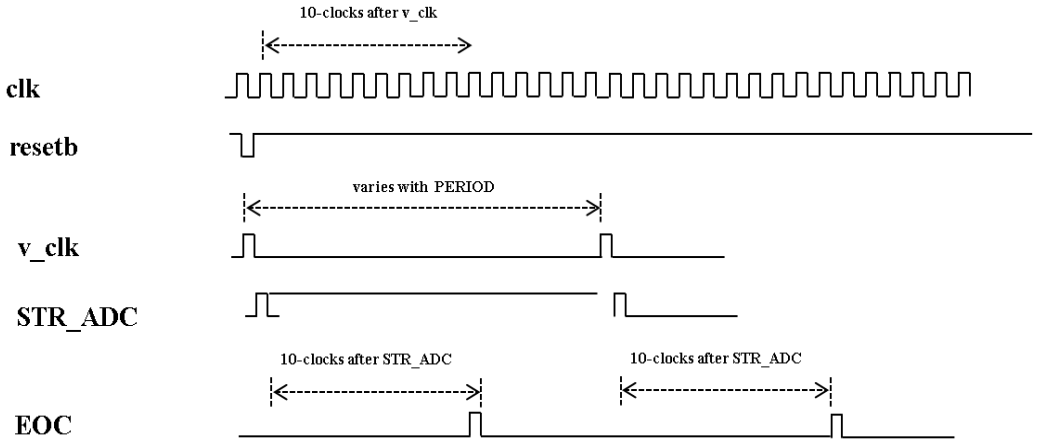


Figure 7. ADC Timing Diagram of Fingerprint LSI

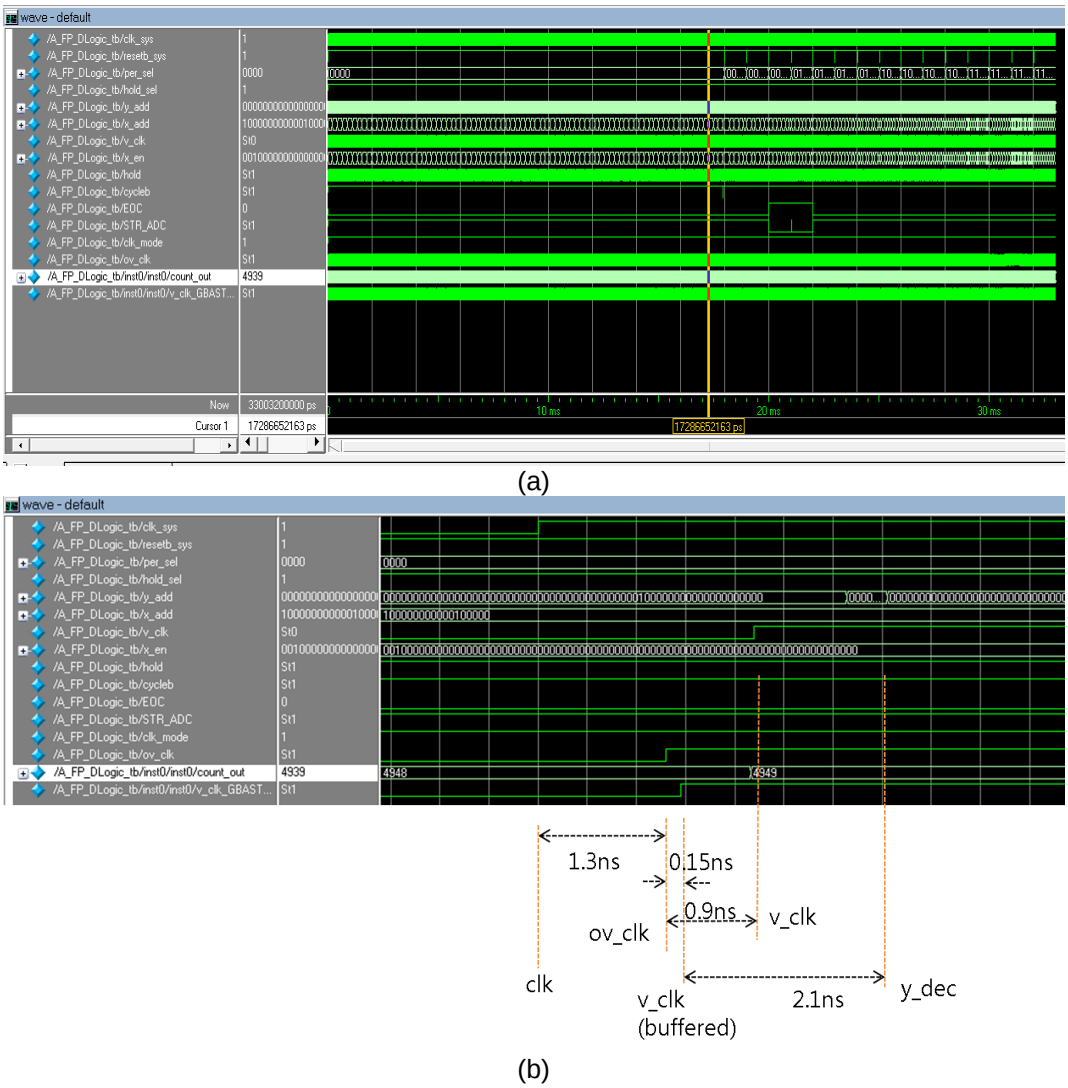


Figure 8. Logic Simulation Result of Fingerprint LSI

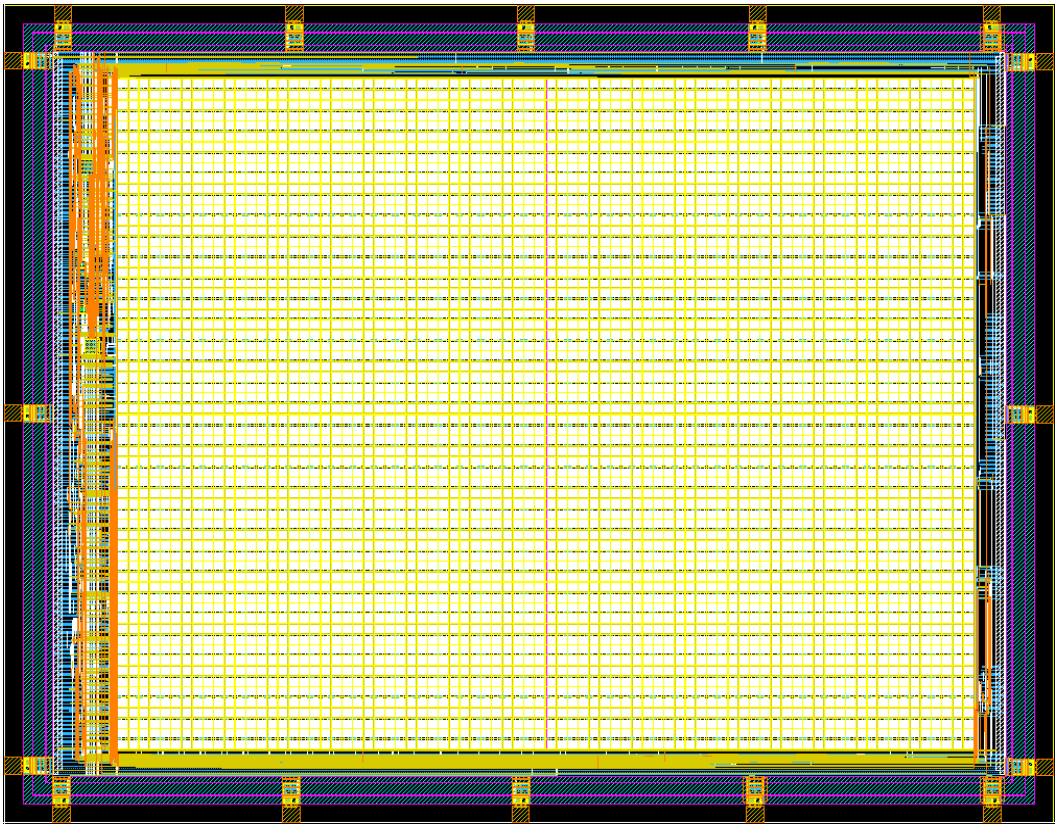


Figure 9. 80 x 64 Pixel Array Chip Layout (4943μm x 3943μm @0.18μm CMOS Process)

4. Conclusion

This paper implements 80x64 array high sensitive fingerprint sensor with the parasitic insensitive charge transfer integrator. The fingerprint sensor cell uses an active output voltage feedback integrator. The detection circuit of one pixel includes a pixel level charge transfer and parasitic insensitive integrator with a differential amplifier with pmos input. A multiple integration scheme is proposed to improve signal-to-noise ratio and amplify the sensing signal, which enables and robust fingerprint sensor driver architecture. The parasitic insensitive charge transfer circuit includes a simple differential amplifier and two switches to remove parasitic capacitance and transfer charge. The operation is validated by HSPICE for one-pixel and RTL simulation including logic synthesis for the full chip design on condition of 0.18μm typical CMOS process and 1.8V power. The voltage difference between a ridge and valley is about 215mV after 10 clock cycles and 367mV after 20 clock cycles. The maximum frequency of cell operation is 10MHz. The simulation results show the parasitic insensitive characteristics which increase touch sensitivity of the circuit. Full chip logic is synthesized and integrated with 80x64 array sensor core. The layout is performed by full custom flow for one-pixel and auto P&R for the full chip. The area of the full chip is 19.5 mm^2 (4943μm x 3943μm) and the gate count is 542,000. The area of one-pixel is 50μm x 50μm. Pitch is 50μm and image resolution is 508dpi.

Acknowledgements

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