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HSTL IO Standards Based Processor Specific Green Counter Design on 90nm FPGAAbhay Saxena

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Abstract

Extending battery life and increase in portability of modern electronic devices and gadgets are the main motives behind the Green Computing which is also known by similar terms like energy efficient design or low power design or green design. Such efficiency is only possible if all the components of processor are also energy efficient. In this work, the researchers tried to analyze the energy optimization possibility in counter design by selection of energy efficient IO standards. The researchers had used High Speed Transceiver Logic for the purpose of energy efficient counter design on Spartan3 (90nm) FPGA (field-programmable gate array) using VHDL (VHSIC Hardware Description Language) hardware description language along with the Xilinx ISE simulator for the analysis and synthesis of counters. Spartan 3 with 90 nm low power is used to achieve substantial power savings. Here, researchers have used five different HSTL IO standards for this work. The standards used are HSTL_I, HSTL_III, HSTL_III_18, HSTL_III_DCI and HSTL_II_18. With these sets of IO standards, Researchers had run their counter design on various device operating frequencies (1.0 GHz to 4.0 GHz). The results clearly indicate that this dynamic frequency (1.0 GHz in lieu of 4.0 GHz) scaling had saved 45% of total power.

Keywords*: IOStandards, HSTL, Environment-Friendly Design, Counter, Energy Efficiency, FPGA*

1. Introduction

Energy efficiency is an important demand to extend the battery life of computing devices. Energy efficient design or green design is the focus behind green computing. Low power or energy efficient process is possible only if all the components of processor are also energy. We also have one small component that we have draw attention to is the Johnson Counter, which is a kind of popular circuit comprises of a series of flip-flops which are connected together in a feedback manner.

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2. Literature Survey on Counter

Counter can be used to count packet in networking, clock pulse in architecture and so on. These days there is research trend in power efficient counter design among researchers. Some are using mapping[1] and some are using HDL coding [2] for same purpose. HSTL IO standards also proved itself as integral part of green design after successful integration of HSTL in green designing of ROM [3] and ALU [4]. Not only HSTL but SSTL IO standards are also in the use of energy efficient design [5]. Research is also going on in the design of energy efficient arithmetic circuits [6]. Along with HSTL and SSTL, there are many other logic families which give significant results in energy efficient design for ECG machine [7]. Along with logic families, voltage scaling's are also well proved techniques for energy efficient counter.

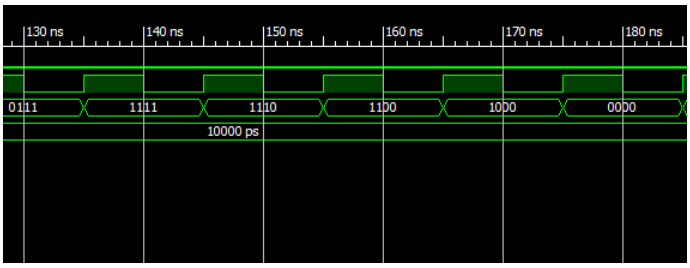

Figure 1. Waveform Configuration of Johnsoncounter

3. Related Work

Green computing is becoming crucial area in the research laboratories today and will be mandatory in very near future. In the engineering research today, a huge amount of work is in progress for designing and development of the alternative devices, algorithms and mechanism to minimize the power consumption by the computing devices. Specifically, a number of research papers have mentioned the breakdown in FPGAs about the dynamic power consumption. The first 90nm FPGA delivering more bandwidth and functions was Spartan3.

Even, in the programmable logic industry, Spartan-3 has set new standards in power savings. It has promoted those applications which have considerably low power footprint and cost sensitive too. The application of this technology is highly usable in various devices such as displays, set-top boxes, wireless routers *etc*. Xilinx is the better example of PGAs, design tools and referencing design. A lot of work is still in progress in the industry as well. HSTL IO standards also proved itself as integral part of green design after successful integration of HSTL in green designing of ROM [3] and ALU [4]. Not only HSTL but SSTL IO standards are also in the use of energy efficient design. Research is also going on in the design of energy efficient arithmetic circuits [6]. So, still today, there is immense need in energy efficient counter design.

Based on the existing work, in this paper researchers want to compare power loss by various High Speed Transceiver Logic versions at different frequencies in counter design on Spartan 3 FPGA using VHDL and Xilinx simulator. Ultimately, by varying the frequencies in various standards we want to observe the static and dynamic power and want to conclude the performance as result for different existing standards.

4. Using Hstl Io Standards For Energy Optimization

In this work, researchers had passed the counter design through the compatibility test with range of device operating frequencies like 1.0GHz, 2.9GHz, 3.3GHz, 3.6GHz,

3.8GHz and 4.0GHz to get the desired result. Various energy efficient techniques are also in practice such as capacitance, voltage, frequency scaling, power gating *etc*. In this work we have used HSTL for energy efficient counter design on 90nm FPGA (Family: Spartan 3, Part: xc3s50, Package: pq208, Temp Grade: Commercial, Speed Grade: -5) using VHDL hardware description language and Xilinx ISE simulator. The researches have further used different six HSTL IO standards which are depicted in the Figure 1 above. These standards used are HSTL_I, HSTL_III, HSTL_III_18, HSTL_III_DCI and HSTL_II_18.

HSTL IO standard is rather used to avoid the reflection of transmission line by comparing the various impedance and ports. What is all important in the overall power dissipation is the selection of HSTL IO standards. We are bit focused on to find the most energy efficient HSTL IO standards for counter designing. Also we have tested the counter's compatibility with the latest i7 processor for better implementation. ROM is being operated with the same frequency as supported by I7 processor (tabulated in Table 1). By using 4610Y, 4600U, 4600M, 4960HQ and 4790K different series of I7 processors, we had opertated on design counter with numerous sets of frequencies (as Table 1).

Table 1. Various I7 Processor and Respective Frequencies

I7 Processor	Frequency	**Cores**
4610Y	2.9GHz	4
4600U	3.3GHz	2
4600M	3.6GHz	2
4960HQ	3.8GHz	2
4970K	4.0GHz	4

We found that the static power remains constant with the IO standard Variations, whereas IO Power changed significantly with varied IO standard.

We all knows that Static and dynamic are two components of power dissipation. The summation of total dynamic and total leakage power is total power. So in next sections we had made power analysis by changes in IO standards with uniform frequency followed by frequency variations with IO standards constant and in last conclusion and future scope of designed is worked out.

5. Power Analysis Using Hstl Io Standard for Different Frequencies

This segment with the use of five different HSTL, the researchers are using varied frequencies from 1.0 GHz to 4.0 GHz range to run our counter design (refer Table 2).

A. *Power Dissipation with HSTL-I IO Standard*

Table 2. Power Dissipation with HSTL_I IO Standard

Power→ Frequency↓	**Static Power**	**Dynamic Power**	**Total Power**
1.0GHz	0.116	0.046	0.162
2.9GHz	0.116	0.132	0.248
3.3GHz	0.117	0.150	0.267
3.6GHz	0.117	0.164	0.280
3.8GHz	0.117	0.173	0.290
4.0GHz	0.117	0.182	0.299

This shows that we can save upto 45.8% total power by operating our device with 1GHz frequency in less peak performance demand. This will be reflected in power saving as shown in Table 2 and figure 2.

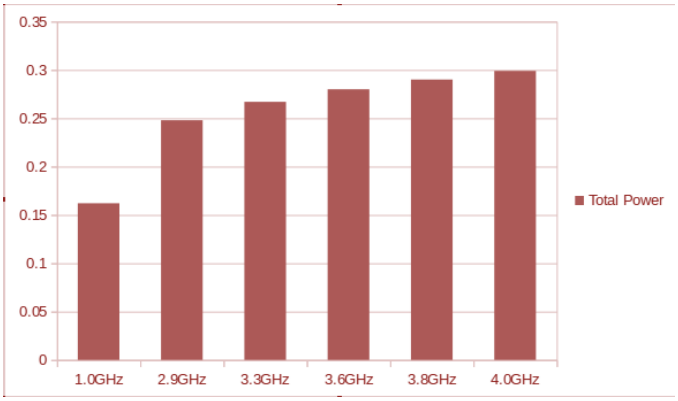

Figure 2. Power Dissipation on Different Frequencies

B. *Power Dissipation with HSTL-III IOStandard*

Table 3. Power Dissipation with HSTL_III IO Standard

Power→ Frequency↓	Static Power	Dynamic Power	Total Power
1.0GHz	0.090	0.063	0.153
2.9GHz	0.091	0.182	0.273
3.3GHz	0.091	0.207	0.298
3.6GHz	0.091	0.226	0.317
3.8GHz	0.091	0.238	0.329
4.0GHz	0.091	0.251	0.342

It is easily observable in Table 3 and Figure 3 that a significant change of 20.17% in total power, if we changed the frequency from 4GHz to 2.9 GHz.

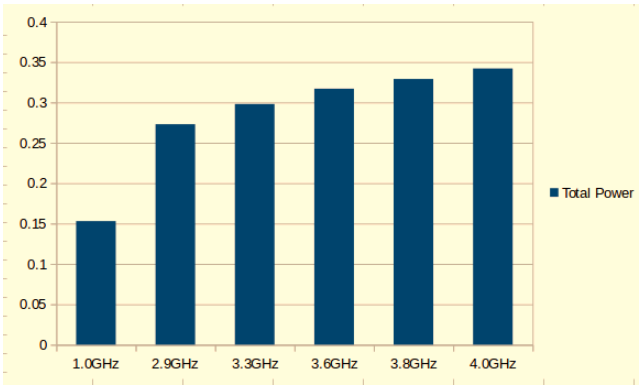

Figure 3. Power Dissipation on Different Frequencies

C. *Power Dissipation with HSTL-III_18 IO Standard*

Table 4. Power Dissipation with HSTL_III_18 IO Standard

Power→ Frequency↓	Static Power	Dynamic Power	Total Power
1.0GHz	0.111	0.073	0.184
2.9GHz	0.112	0.210	0.322
3.3GHz	0.112	0.239	0.351
3.6GHz	0.112	0.261	0.373
3.8GHz	0.112	0.275	0.387
4.0GHz	0.112	0.290	0.402

It is clearly visible from Table 4 and Figure 4 that there is a change of 12.67% in total power by varying the frequencies.

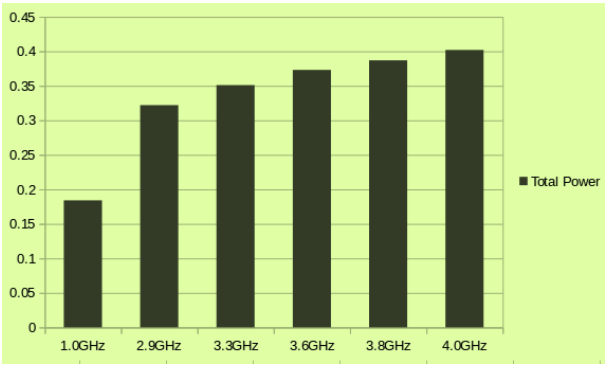

Figure 4. Power Dissipation on Different Frequencies

D. *Power Dissipation with HSTL_III_DCI IOStandard*

Table 5. Power Dissipation with HSTL_III_DCI Iostandard

Power→ Frequency↓	Static Power	Dynamic Power	Total Power
1.0GHz	0.069	0.064	0.133
2.9GHz	0.070	0.184	0.254
3.3GHz	0.070	0.210	0.279
3.6GHz	0.070	0.229	0.299
3.8GHz	0.070	0.241	0.311
4.0GHz	0.070	0.254	0.324

Figure 5 and Table 5 shows that with the variation of frequencies from 4 GHz to 3.6 GHz, the total power is 7.71% changed.

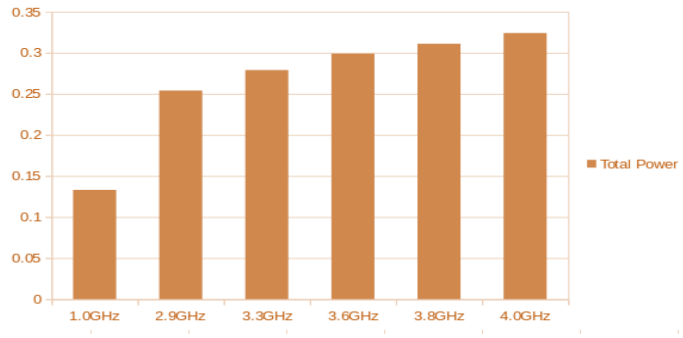

Figure 5. Different Frequencies and Power Dissipation

E. *Power Dissipation with HSTL_II_18 IO Standard*

Table 6.Power Dissipation with Hstl_Ii_18 Io Standard

Power→ Frequency↓	Static Power	Dynamic Power	Total Power
1.0GHz	0.195	0.039	0.235
2.9GHz	0.195	0.114	0.309
3.3GHz	0.196	0.130	0.325
3.6GHz	0.196	0.141	0.337
3.8GHz	0.196	0.149	0.345
4.0GHz	0.196	0.157	0.353

Table 6 and Figure 6 shows the change in 2.27% total power changes if the frequency changes from 4 GHz to 3.8 Ghz.

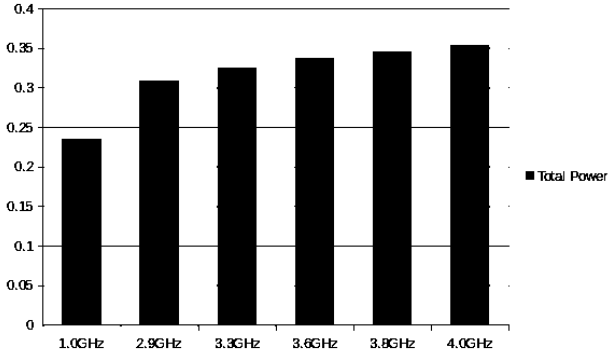

Figure 6. Power Dissipation on Different Frequencies

5. Power Analysis of Counter for Different Hstl

After analyzing the various power performances with varied frequencies, now we will work out with various HSTL standards with fixed frequency (Case 1 to 6).

Case 1. *On 1 GHz Device Operating Frequency*

Power→ HSTL↓	Static Power	Dynamic Power	Total Power
HSTL_I	0.116	0.046	0.162
HSTL_III	0.090	0.063	0.153
HSTL_III_18	0.111	0.073	0.184
HSTL_III_DCI	0.069	0.064	0.133
HSTL_II_18	0.195	0.039	0.235

Table 7.Power Dissipation with Different HSTL

With the static power unchanged but HSTL_II_18 had 31.06%, 34.89%, 21.70% and 43.40% more total power consumption compared to various other HSTL at 1 GHz (Table 7, Figure 7)

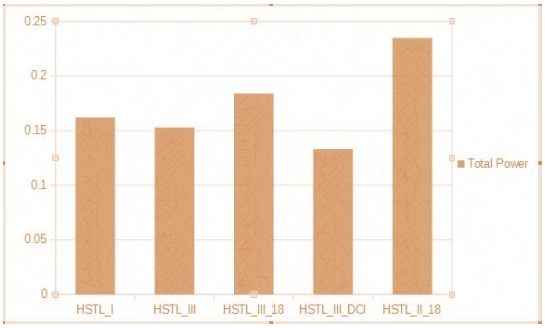

Figure 7. Different Variants Of HSTL and Power Dissipation

Case 2. *On 2.9GHz Device Operating Frequency*

Table 8.Variant HSTL and Power Dissipation

Power→ HSTL↓	Static Power	Dynamic Power	Total Power
HSTL_I	0.116	0.132	0.248
HSTL_III	0.091	0.182	0.273
HSTL_III_18	0.112	0.210	0.322
HSTL_III_DCI	0.070	0.184	0.254
HSTL_II_18	0.195	0.114	0.309

Table 8 and Figure 8 shows that at 2.9 GHz the HSTL_III_18 had 22.98%, 15.21%, 21.11% and 4.04% more total power consumption compare to HSTL_I, HSTL_III, HSTL_III_DCI and HSTL_II_18 respectively

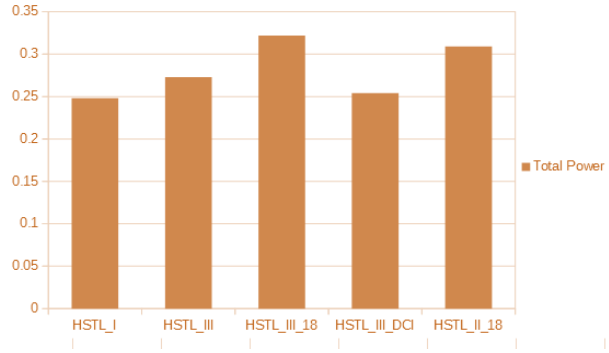

Figure 8. For Frequency 2.9 GHz

Case 3. *On 3.3 GHz Device Operating Frequency*

Table 9. Power Dissipation with Different HSTL

Power→ HSTL↓	Static Power	Dynamic Power	Total Power
HSTL_I	0.117	0.150	0.267
HSTL_III	0.091	0.207	0.298
HSTL_III_18	0.112	0.239	0.351
HSTL_III_DCI	0.070	0.210	0.279
HSTL_II_18	0.196	0.130	0.325

For static frequency 3.3 GHz, HSTL_III_18 had 23.93%, 15.10%, 20.51% and 7.40% more total power consumption as compared to other variants of HSTL (Table 9 and Figure 9).

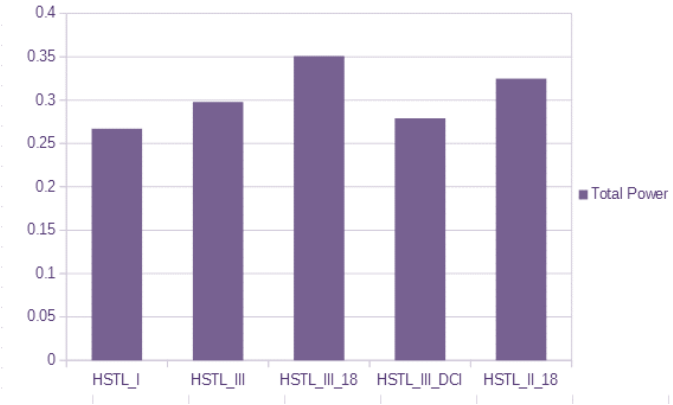

Figure 9. For Frequency 3.3 GHz

Case 4. *On 3.6 GHZ Device Operating Frequency*

Table 10. Power Dissipation with Different HSTL

Power→ HSTL↓	Static Power	Dynamic Power	Total Power
HSTL_I	0.117	0.164	0.280
HSTL_III	0.091	0.226	0.317
HSTL_III_18	0.112	0.261	0.373
HSTL_III_DCI	0.070	0.229	0.299
HSTL_II_18	0.196	0.141	0.337

At static frequency 3.6 GHz, the HSTL_III_18 had 24.93%, 15.01%, 19.84% and 9.65% more total power consumption as compared to other HSTL variants respectively. (Table 10 and Figure 10)

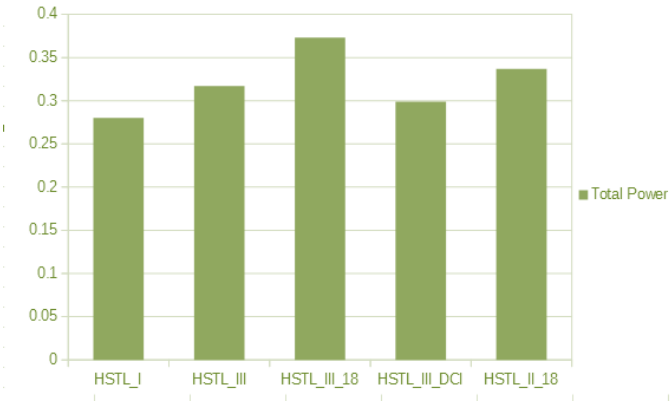

Figure 10. For Frequency 3.6 Ghz

Case 5. On 3.8 GHz *Device Operating Frequency*

Table 11. Power Dissipation with Different HSTL

Power→ HSTL↓	Static Power	Dynamic Power	Total Power
HSTL_I	0.117	0.173	0.290
HSTL_III	0.091	0.238	0.329
HSTL_III_18	0.112	0.275	0.387
HSTL_III_DCI	0.070	0.241	0.311
HSTL_II_18	0.196	0.149	0.345

The static power remained unchanged when frequency was 3.8 GHz but HSTL_III_18 had 25.06%, 14.99%, 19.64% and 10.85% more total power consumption with HSTL_I, HSTL_III, HSTL_III_DCI and HSTL_II_18 (Table 11 and Figure 11).

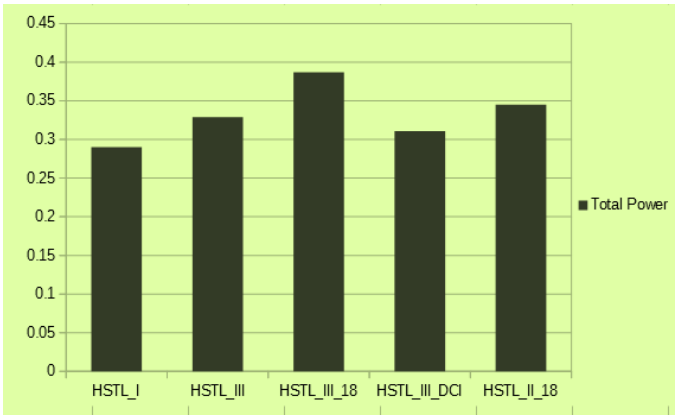

Figure 11. For 3.8 GHz

Case 6. *On 4.0 GHz Device Operating Frequency*

Table 12. Power Dissipation with Different HSTL

Power→ HSTL↓	Static Power	Dynamic Power	Total Power
HSTL_I	0.117	0.182	0.299
HSTL_III	0.091	0.251	0.342
HSTL_III_18	0.112	0.290	0.402
HSTL_III_DCI	0.070	0.254	0.324
HSTL_II_18	0.196	0.157	0.353

At Frequency 4.0 GHz, there was no change in static power but HSTL_III_18 had 25.62%, 14.93%, 19.40% and 12.19% more total power consumption in compared to other Varied HSTL. (Table 12 and Figure 12)

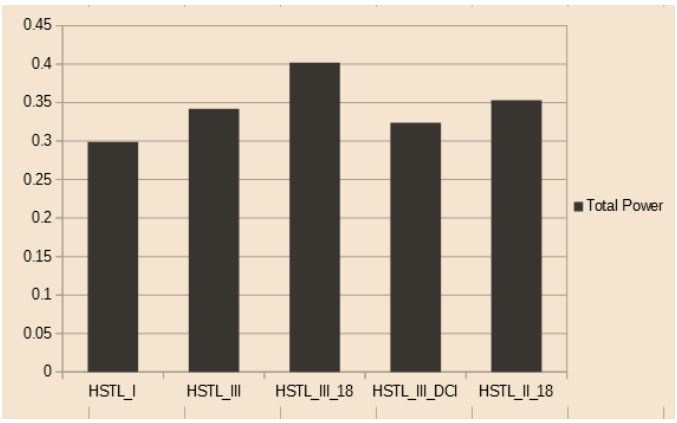

Figure 12. For 4.0 GHz

7. Conclusion

The authors compared power loss by change in high speed transceiver logic versions at varied frequencies in counter design on Spartan 3FPGA using VHDL and Xilinx ISE

simulator. With six devise operating frequencies (ranging from 1.0 GHz to 4.0 GHz), the counter design had passed the compatibility test. Under dynamic frequency scaling, they were scaled down to 4.0 GHz to 1.0 GHz. It was observed that although there is no significant change in static power, the HSTL_III_18 had higher power consumption and HSTL_I was the least power consumer.

8. Future Scope

Green computing is supposed to be for more and more power saving, battery life and easily portability. There are various energy efficient techniques like clock gating, clock enable, capacitive and voltage scaling, power gating where this work can also be easily carried out. It can also be enhanced by using new FPGA families and can be implemented to 28nm, 40 nm and 90 nm FPGA.

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