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Analysis of Thermal Stability of Energy Efficient Arithmetic Circuit Design on Different FPGA

Sehra Jindal, Prabhdeep Singh, Shreya Goel, Vivek Guraba,

Chitkara University
Punjab, India
{sehrajindal6, deepprabh95, shreyagoelsg}@gmail.com, vguraba@hotmail.com,

Abstract

The paper involves discovering how the power dissipation of arithmetic circuits on FPGAs changes with the ambient temperature. We have covered 90nm, 65nm, 45nm, 40nm and 28nm technology based FPGA. The goal of the paper is to analyze the Power dissipation of arithmetic circuits on 23 FPGAs for 4 different temperatures. This has been done by checking the power dissipation of FPGAs by connecting them to XPower Analyzer which is a utility for estimating the power consumption and junction temperature of FPGA devices. The devices were connected to the XPower Analyzer which calculated power dissipation on different temperature as well as the total average power consumption and generated a report. Also the Percentage reduction in power when ambient temperature is scaled down is calculated. We are getting 20-90% reduction in power consumption, when we are using the most energy efficient FPGA available.

Keywords: *arithmetic circuits, FPGA, power dissipation, reduction in power*

1. Introduction

In FPGA based arithmetic design, there are FPGA based ALU using rapid prototyping [1], 32 Bit Hybrid Carry Propagate Adder with Efficient Hardware Resource in FPGA [2], design and implementation of floating point ALU [3], High Speed Carry Save Multipliers [4], Drive Strength and LVCMOS Based energy efficient ALU design on FPGA [5], Mapping based Low Power ALU design [6], Clock Gating Aware Low Power ALU [7], and Mobile DDR IO standard based high performance energy efficient portable ALU [10]. Arithmetic circuits are known to perform various arithmetic tasks, the most basic of them being addition and subtraction. A binary adder-subtractor is a combinational circuit that performs the arithmetic operation on the input provided in the form of binary bits. A FPGA is an integrated circuit which can be configured later on by the user. The FPGA configuration is generally specified using a hardware description language (HDL). FPGAs have come to rival corresponding application specific devices by having the upper hand in terms of power, speed, economic efficiency and increased reusability.

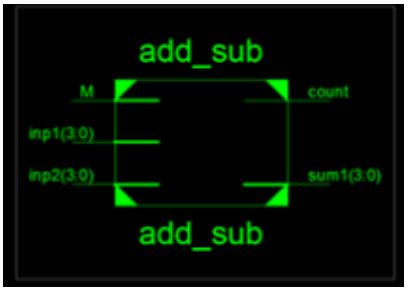

Figure 1. Top Level Schematic of Arithmetic Circuit Design

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The arithmetic circuit takes 3 inputs, provides 2 outputs and the operation addition and subtraction depends on the value of M. The power dissipation of arithmetic circuits on 23 FPGA (Field programmable gate array) for 4 different temperatures was calculated using XPower Analyzer. The percentage power reduction after scaling down the ambient temperature from 348.15K to 323.15K, 298.15K and 273.15K was also calculated as shown in Figure 2. We have covered 90nm, 65nm [9], 45nm, 40nm and 28nm technology based FPGA.

Table 1. Different FPGA Used to Verify Thermal Stability& Energy Efficiency

Artix-7	Kintex-7 Low Voltage
Artix-7 Low Voltage	Spartan-3A DSP
Automotive Artix-7	Spartan-3
Automotive Spartan-3A DSP	Spartan-3A and Spartan-3AN
Automotive Spartan-3	Spartan-3E
Automotive Spartan-3A	Spartan-6
Automotive Spartan-3E	Spartan-6 Lower Power
Automotive Spartan-6	Virtex4
Automotive Zynq	Virtex5
Defense-Grade Artix-7	Virtex6 Lower Power
Defense-Grade Artix-7 Low Voltage	Zynq
Kintex-7	

As shown in Table 1, there are 23 different FPGAs selected for this experiment to test thermal stability and energy efficiency of our arithmetic circuits design. We have cover ed 90nm technology based FPGA, 65nm technology based FPGA, 45nm technology based FPGA, 40nm technology based FPGA, and 28nm technology based FPGA. For same process technology based FPGA, we have taken automotive, defense and normal FPGA. Zynq, Artix-7 and Kintex-7 are 28nm technology based FPGA. Spartan-3 and Virtex-4 are 90nm technology based FPGA. Virtex-5 are 65nm technology based FPGA and Virtex-6 is 40nm technology based whereas 45nm technology is used for fabrication of Spartan-6.

3. Observations and Results

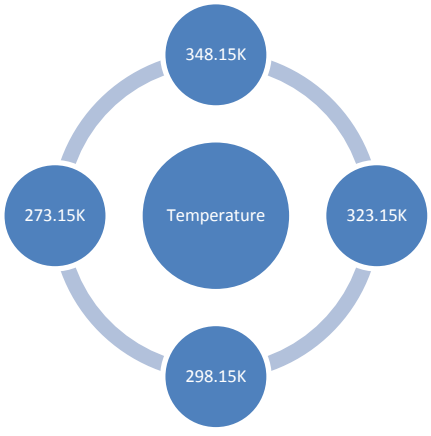

Figure 2. Different Ambient Temperature Used To Test Thermal Stability of Design

3.1 On Artix-7, Artix-7 Low Voltage, Automotive Artix-7, Automotive Spartan-3 A DSP, Automotive and Spartan-3 FPGA

Table 2. Power Dissipitation of Arithmetic Circuits for Different Temperature

	273.5 K	298.15K	323.15K	348.15K
Artix-7	0.03	0.042	0.075	0.166
Artix-7 Low Voltage	0.029	0.037	0.062	0.13
Automotive Artix-7	0.03	0.042	0.075	0.166
Automotive Spartan-3A DSP	0.098	0.114	0.138	0.174
Automotive Spartan-3	0.025	0.027	0.03	0.034

As shown in Table 2, Spartan-3A DSP is the worst power consumer and Spartan-3 are the most energy efficient FPGA. Artix-7 is 28nm technology based FPGA whereas 90nm technology is used in fabrication of Spartan-3. The percentage (%) reduction in power after scaling down the surrounding temperature from 348.15K to 323.15K is of [(0.166-0.075)/0.166]*100=54.81%, 298.15K is of [(0.166-0.042)/0.166]*100=74.69% and 273.15K of [(0.166-0.03)/0.166]*100=81.92% on *Artix-7* as shown in Table 2 and Figure 3. But on *Artix-7 Low Voltage* the percentage (%) reduction in power on lowering the ambient temperature from 348.15K to 323.15K is [(0.13-0.062)/0.13]*100=52.30%, 298.15K is [(0.13-0.037)/0.13]*100=71.53% and 273.15K is [(0.13-0.029)/0.13]*100=77.69%. And on *Automotive Artix-7* percentage (%) reduction in power after scaling down the surrounding temperature from 348.15K to 323.15K is [(0.166-0.075)/0.166]*100=54.81%, 298.15K is [(0.166-0.042)/0.166]*100=74.69% and 273.15K is [(0.166-0.03)/0.166]*100=81.92%. For *Automotive Spartan-3A DSP* percentage (%) reduction in power when we lowered the ambient temperature from 348.15K to 323.15K is [(0.174-0.138)/0.174]*100=20.68%, 298.15K is [(0.174-0.114)/0.174]*100=34.48% and 273.15K is [(0.174-0.098)/0.174]*100=43.67%.Similarly percentage (%) reduction in power when we bring down ambient temperature from 348.15K to 323.15K is of [(0.034-0.03)/0.034]*100=11.76%, 298.15K is of [(0.034-0.027)/0.034]*100=20.58% and 273.15K is of [(0.034-0.025)/0.034]*100=26.47% on *Automotive Spartan-3.*

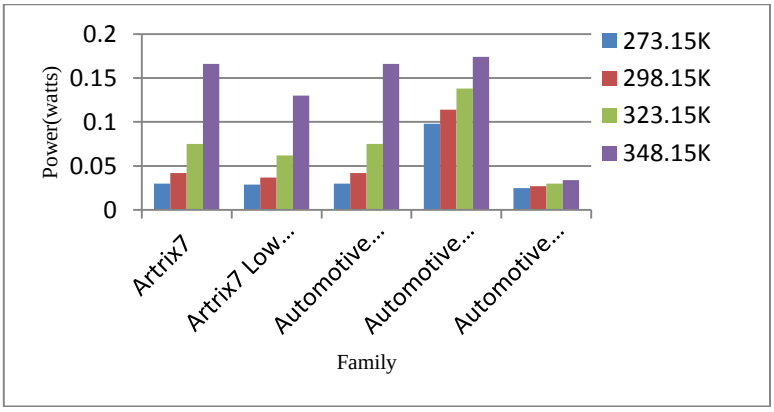

Figure 3. Power Dissipation On 5 Different FPGA And 4 Different Temperatures

3.2 On Automotive Spartan-3 A, Automotive Spartan-3 E, Automotive Spartan-6, Automotive Zynq, and Defense-Grade Artix-7 FPGA

Table 3. Power Dissipation of Arithmetic Circuits For Different Temperature

	273.15 K	298.15 K	323.15 K	348.15 K
Automotive Spartan-3A	0.014	0.017	0.021	0.027
Automotive Spartan-3E	0.03	0.034	0.038	0.045
Automotive Spartan-6	0.009	0.014	0.023	0.042
Automotive Zynq	0.05	0.063	0.101	0.189
Defense-Grade Artix-7	0.03	0.042	0.075	0.166

We are using 90nm technology based Spartan-3, 45nm technology based Spartan-6 and 28nm technology based Zynq and Artix-7 FPGA as shown in Table 2 and Figure 3. There is percentage (%) reduction in power after scaling down the ambient temperature from 348.15K to 323.15K of [(0.027-0.021)/0.027]*100=22.22%, 298.15K of [(0.027-0.017)/0.027]*100=37.03% and 273.15K of [(0.027-0.014)/0.027]*100=48.14% on *Automotive Spartan-3A*. Whereas the percentage (%) reduction in power when we lower the temperature from 348.15K to 323.15K is [(0.045-0.038)/0.045]*100=15.55%, 298.15K is[(0.045-0.034)/0.045]*100=24.44% and 273.15K is [(0.045-0.03)/0.045]*100=33.33% on *Automotive Spartan-3E*. But percentage (%) reduction in power on lowering the ambient temperature from 348.15K to 323.15K is [(0.042-0.023)/0.042]*100=45.23%, 298.15K is [(0.042-0.014)/0.042]*100=66.66% and 273.15K is [(0.042-0.009)/0.042]*100=78.57% on *Automotive Spartan-6.* Also the percentage (%) reduction in power on bringing down ambient temperature from 348.15K to 323.15K is of [(0.189-0.101)/0.189]*100=46.56%, 298.15K is of [(0.189-0.063)/0.189]*100=66.66% and 273.15K is of [(0.189-0.05)/0.189]*100=73.54% on *Automotive Zynq*. But for *Defense Grade Artix-7* the percentage (%) reduction in power after scaling down surrounding temperature from 348.15K to 323.15K is [(0.166-0.075)/0.166]*100=54.81%, 298.15K is [(0.166-0.042)/0.166]*100=74.69% and 273.15K is [(0.166-0.03)/0.166]*100=81.92% as shown in Table 3 and Figure 4. Zynq is the worst power consumer and Spartan-6 is the most energy efficient FPGA.

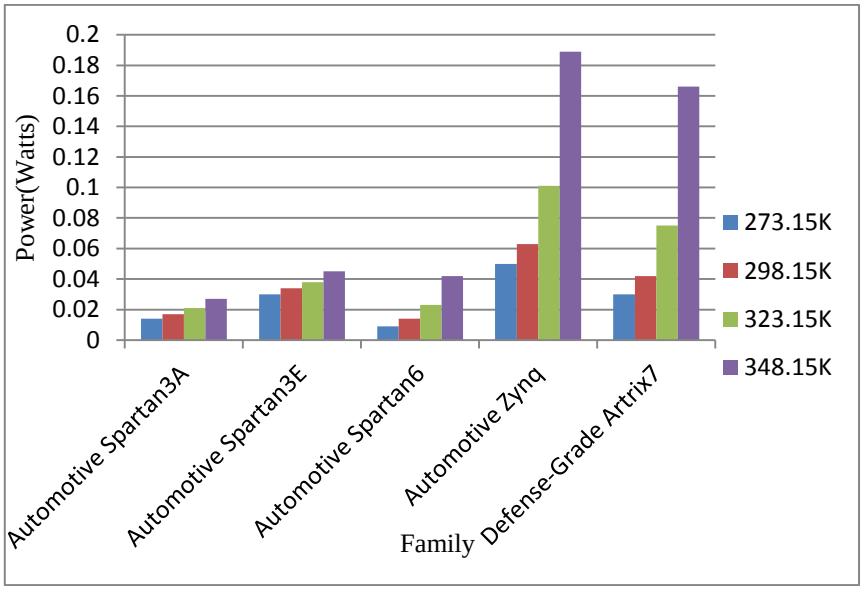

Figure 4. Power Dissipation on 5 Different FPGA And 4 Different Temperatures

3.3 On Defense-Grade Artix-7 Low Voltage, Kintex-7, Kintex-7 Low Voltage, Spartan-3 A DSP, and Spartan-3 FPGA

Table 4. Power Dissipation of Arithmetic Circuits For Different Temperature

	273.15K	298.15K	323.15K	348.15K
Defense-Grade Artix-7 Low Voltage	0.03	0.042	0.075	0.166
Kintex-7	0.029	0.045	0.088	0.207
Kintex-7 Low Voltage	0.027	0.039	0.07	0.156
Spartan-3A DSP	0.156	0.114	0.138	0.174
Spartan-3	0.025	0.027	0.03	0.034

We are using 28nm technology based Artix-7 and Kintex-7 FPGA and 90nm technology based Spartan-3 FPGA. There is following percentage (%) reduction in power on bringing down ambient temperature from 348.15K to 323.15K of [(0.166-0.075)/0.166]*100=54.81%, 298.15K of [(0.166-0.042)/0.166]*100=74.69% and 273.15K of [(0.166-0.03)/0.166]*100=81.92% on *Defense Grade Artix-7 Low Voltage*. As far as *Kintex-7* is concerned the percentage (%) reduction in power on lowering down surrounding temperature from 348.15K to 323.15K is of [(0.207-0.088)/0.207]*100=57.48%, 298.15K is of [(0.207-0.045)/0.207]*100=78.26% and 273.15K is of [(0.207-0.029)/0.207]*100=85.99%. As per calculation the percentage (%) reduction in power when we scaled down temperature from 348.15K to 323.15K is of [(0.156-0.07)/0.156]*100=55.12%, 298.15K is of [(0.156-0.039)/0.156]*100=75.00% and 273.15K is of [(0.156-0.027)/0.156]*100=82.69% on *Kintex-7 Low Voltage*. The percentage (%) reduction in power on *Spartan-3A DSP* on scaling down surrounding temperature from 348.15K to 323.15K is of [(0.174-0.138)/0.174]*100=20.68%, 298.15K is of [(0.174-0.114)/0.174]*100=34.48% and 273.15K is of [(0.174-0.098)/0.174]*100=43.67%. For *Spartan-3* percentage (%) reduction in power on bringing down ambient temperature from 348.15K to 323.15K is of [(0.034-0.03)/0.034]*100=11.76%, 298.15K is of [(0.034-0.027)/0.034]*100=20.58% and 273.15K is of [(0.034-0.025)/0.034]*100=26.47% as shown in Table 4 and Figure 5. Spartan-3A DSP is the most power hungry and Spartna-3 is the least power consumer FPGA.

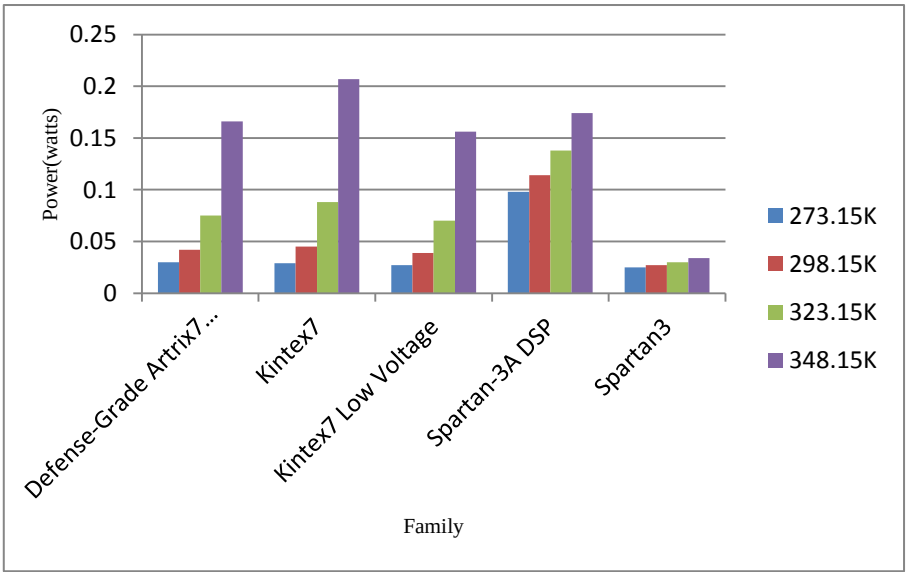

Figure 5. Power Dissipation On 5 Different FPGA And 4 Different Temperatures

3.4 On Spartan-3 A and Spartan-3 AN, Spartan-3 E, Spartan-6, Spartan-6 Lower Power, and Virtex4 FPGA

Table 5. Power Dissipation of Arithmetic Circuits For Different Temperature

	273.15 K	298.15 K	323.15 K	348.15 K
Spartan-3A and Spartan-3AN	0.01	0.01	0.012	0.013
Spartan-3E	0.03	0.034	0.038	0.045
Spartan-6	0.009	0.015	0.023	0.042
Spartan-6 Lower Power	0.008	0.011	0.017	0.028
Virtex4	0.12	0.139	0.166	0.207

In this work, we have taken 90nm technology based Spartan-3 FPGA and 45nm Technology based Spartan-6 along with 90nm technology based Virtex-4 FPGA. Low power version of any FPGA takes less power in compare to other FPGA of the same family. There is percentage (%) reduction in power when we scale down surrounding temperature from 348.15K to 323.15K of [(0.013-0.012)/0.013]*100=7.69%, 298.15K of [(0.013-0.01)/0.013]*100=23.07% and 273.15K of [(0.013-0.01)/0.013]*100=23.07% on *Spartan-3A and Spartan-3AN*. Calculation reveals that percentage (%) reduction in power on reducing down the ambient temperature from 348.15K to 323.15K is of [(0.045-0.038)/0.045]*100=15.55%, 298.15K is of [(0.045-0.034)/0.045]*100=24.44% and 273.15K is of [(0.045-0.03)/0.045]*100=33.33% on *Spartan-3E*. Also for *Spartan-6* the percentage (%) reduction in power on scaling down surrounding temperature from 348.15K to 323.15K is of [(0.042-0.023)/0.042]*100=45.23%, 298.15K is of [(0.042-0.015)/0.042]*100=64.28% and 273.15K is of [(0.042-0.009)/0.042]*100=78.57%. The percentage (%) reduction in power when we scaled down ambient temperature from 348.15K to 323.15K is of [(0.028-0.017)/0.028]*100=39.28%, 298.15K is of [(0.028-0.011)/0.028]*100=60.71% and 273.15K is of [(0.028-0.008)/0.028]*100=71.42% on *Spartan-6 Low Power*. But for *Virtex4* the percentage (%) reduction in power on getting down ambient temperature from 348.15K to 323.15K is of [(0.207-0.166)/0.207]*100=19.80%, 298.15K is of [(0.207-0.139)/0.207]*100=32.85% and 273.15K is of [(0.207-0.12)/0.207]*100=42.02% as shown in Table 5 and Figure 6.

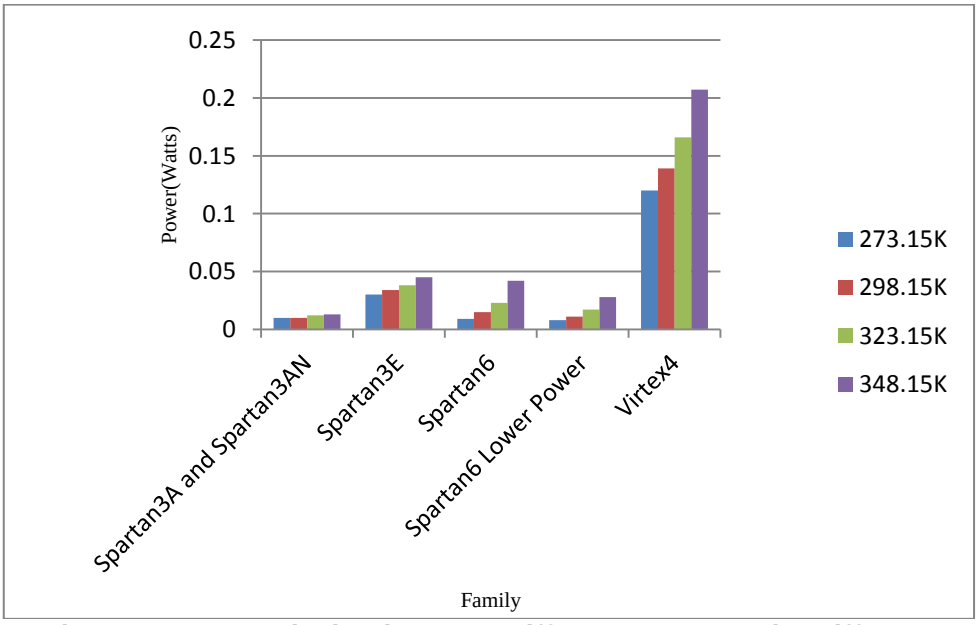

Figure 6. Power Dissipation on 5 Different FPGA And 4 Different Temperatures

3.5 On Virtex5, Virtex6 Lower Power, and Zynq FPGA

Table 6. Power Dissipation of Arithmetic Circuits For Different Temperature

	273.15 K	298.15 K	323.15 K	348.15 K
Virtex5	0.191	0.243	0.321	0.438
Virtex6 Lower Power	0.877	0.956	1.065	1.219
Zynq	0.05	0.065	0.101	0.189

The percentage (%) reduction in power when we brought down surrounding temperature from 348.15K to 323.15K is of [(0.438-0.321)/0.438]*100=26.71%, 298.15K is of [(0.438-0.243)/0.438]*100=44.52% and 273.15K is of [(0.438-0.191)/0.438]*100=56.39% on *Virtex5*. But on *Virtex6 Lower Power* the percentage (%) reduction in power on letting ambient temperature fall from 348.15K to 323.15K is of [(1.219-1.065)/1.219]*100=12.63%, 298.15K is of [(1.219-0.956)/1.219]*100=21.57% and 273.15K is of [(1.219-0.877)/1.219]*100=28.05% . And percentage (%) reduction in power on decreasing temperature from 348.15K to 323.15K is of [(0.189-0.101)/0.189]*100=46.56%, 298.15K is of [(0.189-0.065)/0.189]*100=65.60% and 273.15K is of [(0.189-0.05)/0.189]*100=73.54% on *Zynq* as shown in Table 6 and Figure 7.

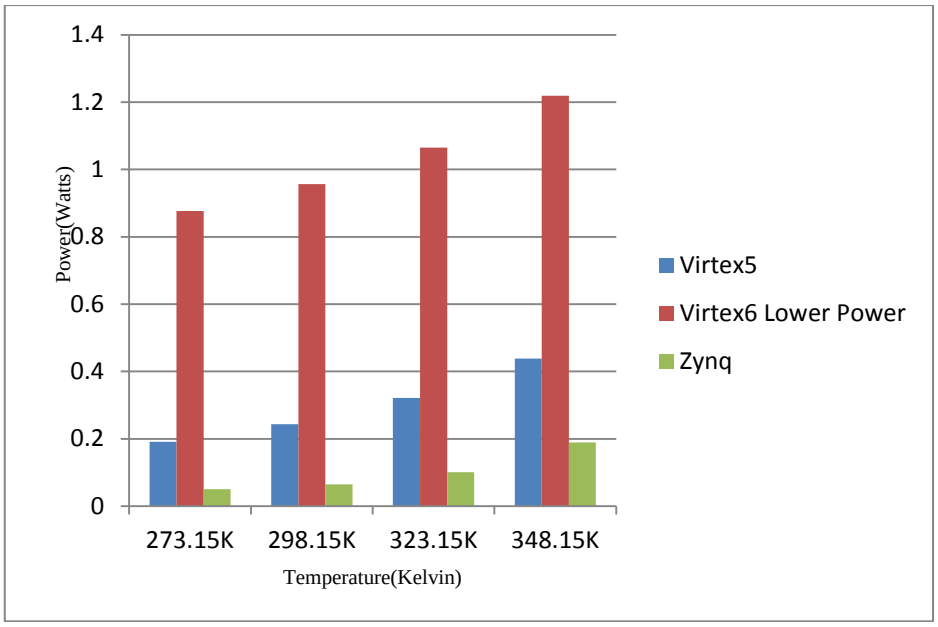

Figure 7. Power Dissipation on 3 Different FPGA And 4 Different Temperatures

4. Conclusion

Arithmetic circuits of addition and subtraction were designed. The power dissipation of arithmetic circuit on 23 FGPA's at 4 different temperatures was calculated using XPower Analyzer. The percentage reduction in power when we scale down the ambient temperature from 348.15K to 323.15K, 298.15.K and 273.15K was calculated taking 348.15K as reference temperature. And it increased with temperature scaling down. So it is possible to say that with the increased temperature, the power dissipation also increased for every FGPA.

5. Future Scope

The flexibility, reconfigurable architecture and cost-effectiveness of FGPAs make them highly desirable for implementation of digital circuits in many industries.

Despite their many advantages FPGAs face problem in power dissipation. It is possible to say that with comparing different FPGAs and the factors affecting their energy efficiency, the problem of power dissipation can be solved thus widening the area of application of FPGA.

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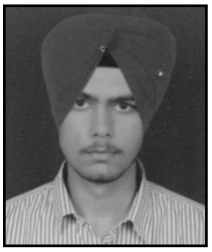
Authors

Sehra Jindal has completed her schooling from Army Public School, Udhampur, Jammu & Kashmir. She is a member of The Institution of Electronics and Telecommunication Engineers (IETE) and is currently doing bachelor of engineering in electronics & communication from Chitkara University, Chandigarh, India.



Prabhdeep Singh was born in Bathinda, Punjab on 25th February 1995. He completed his schooling from G.M.S.S.S., Sec-37B, Chandigarh. He is a member of The Institution of Electronics and Telecommunication Engineers (IETE) and is currently doing his bachelor of engineering in electronics & communication fromChitkara University, Chandigarh, India.

Vivek Guraba was born in Rajpura, Punjab on 19th November 1994. He completed his schooling from Holy Angels School, Rajpura. He is a member of The Institution of Electronics and Telecommunication Engineers (IETE) and is currently doing his bachelor of engineering in electronics & communication from Chitkara University, Chandigarh, India.

Shreya Goel was born in Ambala, Haryana on 12th November 1994. She completed her schooling from Convent of Jesus & Mary, Ambala. She is a member of The Institution of Electronics and Telecommunication Engineers (IETE) and is currently doing her bachelor of engineering in electronics & communication from Chitkara University, Chandigarh, India.