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I/O StandardsBased on Green Communication UsingFibonacci GeneratorDesign on FPGA

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Abstract

In this paper LVCMOS, HSLVDCI, HSTL, LVDCI_DV2 and SSTL Input/output standard is used for the design of Green Fibonacci generator on 40nm FGPA to generate key for Wi-Fi Protected Access in order to make energy efficient communication. In naming convention of I/O standard, LV is low voltage, HS is high speed, DV2 is half impedance, CMOS is Complementary metal Oxide Semiconductor, DCI is digitally control impedance and SSTL is Stub series Transistor Logic. Here we used two frequencies ranging i.e. 1GHz and 10 GHz. After comparison it is observed that, LVDCI-DC2 is the most energy efficient and SSTL15 is the worst energy efficient on 1GHZ frequency where as SSTL15 and HSTL outperforms better on frequency range 10GHz. There is reduction in I/O power requirement of LVDCI is19.19% as compared to SSTL15 and SSTL15 shows 17.60 % reduction in energy on 10GHz as compared to LVDCI-DC2.

Keywords: *I/O standard, LVCMOS, HSTL, SSTL, LVDCI_DV2, Fibonacci Generator, I/O Power, FPGA*

1. Introduction

We used five different I/O standards technique for power efficient Fibonacci generator and it is implemented on virtex-6 FGPA, FF484 packages and XC6VLX75T device. WPA and WPA2 (Wi-Fi Protected Access) key generation can be accomplished by using Fibonacci generator [11]. Where 17-flip-flops, 18 multiplexer and DE multiplexer, one 18 bit adder is used in the Fibonacci generator. The reference voltage for HSLVDCI is 0.75v whereas, HSTL, LVCMOS use 1.2v and, SSTL15 and LVDCI-DC2 with 1.5v.Xpower analyzer is used for power analysis. In earlier [2] we have observed that using SSTL IO standard family to generate a unique 16-bit key using FPGA has been successfully achieved and shows out of all SSTL standards for bidirectional transmission SSTL15 has shown around 70% of reduction in energy dissemination while operating on different frequency ranging from 1GHz to 1THz and given new direction for green communication also.In [2] this while comparing the parameters we have considered three main

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parameters that are Clock, signal and IO power prime focus. Where as in this paper we have extended this work using this with different IO standards in FPGA but for generating 64-bit unique key using Fibonacci generator with two different frequency i.e. 1GHZ and 10GHz, where we also change our prime focus of comparison on basis of IO power only.

2. Literature Review

In [2], the main work was done on six different available classes of Stub-Series Terminated Logic (SSTL) Input/output standard is used for the design of Green Fibonacci generator on 40nm FGPA bidirectional termination. Where it is analysed that SSTL 15 is most energy efficient and saves around is 77.00%, 45.89%, 19.23% and 14.41%energy as compared to other SSTL family standards respectively. In [3], earlier work is done on Digitally Controlled Impedance (DCI) and there is 50% dynamic power reduction at 1.5Vcco, 35.2% dynamic power reduction in DCI based IO standard implementation of RAM seen. We are implementing that work from RAM to Fibonacci generator with different IO standards. In [3], it has been seen around 67% dynamic power reduction with LVCMOS12 when we migrate from 90-nm Spartan-3 FPGA (Field Programmable Gate Array) to 40-nm Virtex-6 FPGA. In [4], LVCMOS I/O standard provides single ended IO interface to the external devices in FPGA, Soc and 3-D IC designs. Reference [5] describes characteristics of the LVCMOS output/input buffer and the design along with challenges at each phase of the design. It describes the other related phenomena e.g. Hot carrier effect, gate oxide integrity is related to the performance of the buffers. The writer of Historia Mathematica in his book interprets Pingala's cryptic formula misrau [**7**]. SSTL is used to design an Image ALU [8] and Fire Sensor [9]. Previously work is done on using SSTL in energy efficient design of Key Generator. In this paper we are comparing different IO standards using two different frequency on 1GHz and 10 GHz and generating energy efficient design key on different frequency and encouraging to work for green communication.

3. Block Diagram of Fibonacci Generator

3.1. Top Level Schematic of Fibonacci Generator

This Fibonacci generator is an energy efficient design using IO standards. The Fibonacci series is invented by Indian mathematician Pingala in 200BC in Taxilla [6]. In this it generate unique 64-bit key using FPGA and help in green communication.

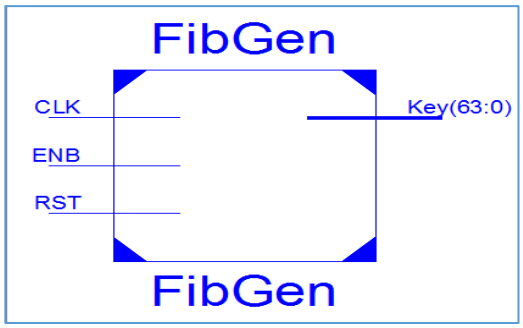

Figure1: Fibonacci Generator Implemented In Xilinx ISE 14.6

Here, we are extending our design approach to five different IO Standards. These are: Low Voltage version of Digitally Controlled Impedance (LVDCI), CMOS (LVCMOS), and Digitally Controlled Impedance Driver with Half Impedance (LVDCI_DV2) and

High Speed version of Low Voltage Digitally Controlled Impedance (HSLVDCI), Transceiver Logic (HSTL).

In Figurer 2, there is input signal clock (CLK), reset (RST), and enable (ENB) signal. There are 64-bit outputs generated by Fibonacci generator in form of each Fibonacci number per clock pulse.

3.2. RTL Schematic of Fibonacci Generator

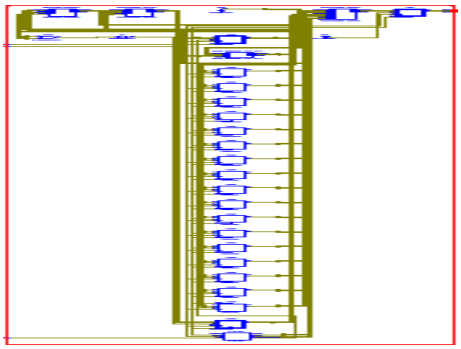

Figure 2: RTL Schematic of Fibonacci Generator

In Figure2, there are one 18-bit adder, two 17-bit 2-to-1 multiplexer, one 64-bit 4-to-1 multiplexer and one Finite State Machine (FSM) in the Register Transfer Level (RTL) schematic of Fibonacci generator.

3.3. Technology Schematic of Fibonacci Generator

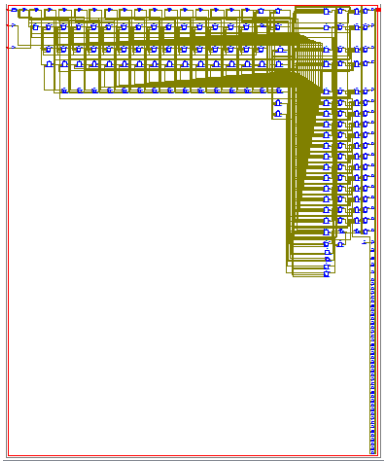

Figure 3: Technology Schematic of Fibonacci Generator

InFigure 3. 71 are Flip-flops/Latches, 1 is Clock Buffers and 66 are input/output Buffers (IO Buffers, one is ground, 74 are look up table (LUT), 18 are multiplexer and 17 are XOR with carry. Out of 71 flip-flops, 20 is D Flip-Flop with Clock Enable and Asynchronous Preset, 50 are D Flip-Flop with Clock Enable and Asynchronous Clear and 1 are D Flip-Flop with Asynchronous Clear. Out of 66 input/output buffers, 2 are input buffer (IBUF) and 64 are output Buffers.

4. RESULTS

A. Low Voltage Digitally Controlled Impedance (LVDCI)

In this we consider readings on two different frequencies 1 GHz and on 10 GHz in which Signal, clock and I/O power are main components of Dynamic power.

Table 1: Power Consumption Using LVDCI-DV2-15

Frequency	*Signal*	*Clock*	*IO*	*Leakage*
1GHz	0.002	0.04	0.10	1.29
10GHz	0.03	0.37	0.88	1.32

I/O power is higher than any other dynamic power and whereas clock power is the least used dynamic power. In Table 1, clock power is 0.036W, 0.35W and I/O power is 0.10W, 0.88W on 1GHz and 10GHz operating frequency respectively.

B. Low Voltage Complementary Mos

Table 2: Power Consumption with LVCOMS15

Frequency	*Signal*	*Clock*	*IO*	*Leakage*
1GHz	0.003	0.04	0.10	1.29
10GHz	0.03	0.36	0.007	1.32

In Table 2, for LVCMOS standards supports 2mA, 4mA, 6mA and 8mA drive current. In this we used LVCMOS15 which support 16mA current. I/O power is 0.10W, 0.007W and Clock power is 0.04W, 0.36W on 1GHz and 10GHz operating frequency respectively.

C. High Speed Transceivers Logic (HSTL)

Table 3: Power Consumption With HSTL_I_18

Frequency	*Signal*	*Clock*	*IO*	*Leakage*
1GHz	0.002	0.04	0.35	1.3
10GHz	0.03	0.36	0.84	1.32

In Table 3, for HSTL standards, I/O power is 0.356W and 0.840W and Clock power is 0.036W, 0.356W on 1GHz and 10GHzoperating frequency respectively.

D. High Speed Lvdci (Hslvdci)

Table 4: Power Dissemination Using HSLVDCI- 18

Frequency	*Signal*	*Clock*	*IO*	*Leakage*
1GHz	0.002	0.04	0.11	1.3
10GHz	0.03	0.40	1.179	1.33

In Table 4, for HSLVDCI-18 standards, I/O power is 0.118W and 1.179W, Clock power is 0.039W and 0.401W on 1GHz and 10GHz operating device frequency respectively.

E. Power Dissipation with SSTL15 I/O Standard

Table 5: Power Dissipation Insstl15

Frequency	*Signal*	*Clock*	*IO*	*Leakage*

1GHz	0.003	0.03	0.21	1.29
10GHz	0.03	0.36	0.57	1.31

In Table 5, for SSTL15 standards, I/O power is 0.216W, 1.577W and Clock power is 0.037W, 0.369W on 1GHz, and 10GHzdevice operating frequency respectively.

F. Effect of IO Standard on IO Power

Table 6: IO Power Calculated By Xilinx Power Analyzer

Frequency	LVCMOS	HSLVDCI	HSTL	LVDCI_DV2	SSTL
1 GHz	0.10	0.11	0.35	0.08	0.21
10GHz	1.00	1.17	0.84	0.88	0.57

A Low voltage Digital Component impedance is taking the minimum IO power which is 8.8mW in quantity. An HSTL input/output standard is taking maximum among all IO standards. We are achieving power reduction in range of -80% using LVDCI_DV2 or LVCMOS in place of SSTL or HSTL as shown in on 1GHz frequency where as

G. Comparison Of Io Standards On 1ghz Frequency

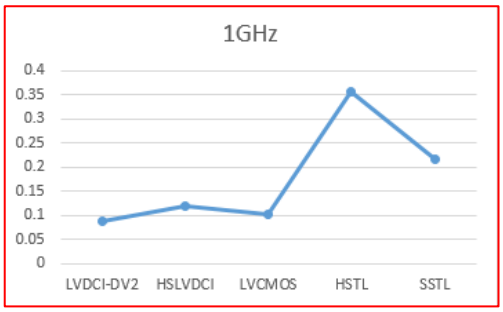

Figure 4: Power Dissipation on 1 Ghz

In Figure 4, by comparing different I/O power of I/O standard, it is observed that, while operating on 1GHz, the reduction in I/O power is19.39%, 20.25%, 33.50%, 19.19% and 21.60% respectively. While studying graph it is observed that LVDCI-DV2 achieve power reduction 81.18% and after that second IO standard which show reduction in power is LVCMOS with nearly 80%. So we can say out of above used IO standard LVDCI-DV2 gives better performance than HSLVDCI, LVCMOS, HSTL and SSTL on frequency used 1GHz.

H. Comparison of Io Standards on 10 Ghz

In Figure 5, On comparing different I/O power it is observed that, while operating on 10 GHz, the reduction in I/O power is 21.79%, 23.47%, 20.25%, 18.19% and 17.60% respectively. From the graph it is observed that SSTL achieve power reduction 82.49% and after that second IO standard which shows reduction in power is HSTL with nearly 80%. So we can say out of above used IO standard SSTL gives better performance than LVDCI-DV2, LVCMOS, HSTL and HSLVDCI on frequency used 10GHz.

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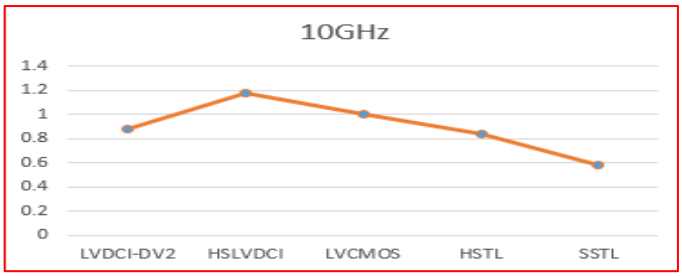

Figure5: Input/Output Comparison Of IO Standards On 10ghz

5. Conclusion

Among 5 different I/O standards, for 1 GHz frequency, LVDCI-DV2 is the most energy efficient and SSTL15 is the worst energy efficient and on comparing the IO standards in 10 GHz, it is observed that SSTL perform better energy efficient when Fibonacci generator is operating with the reduction in I/O power is 17.50% as compare to others.

6. Future Scope

There is an open scope to redesign this Fibonacci generator on 28nm or 16nm ultra scale in order to reduce the power Dissipation. In this work, five different/O standards are used to achieve energy efficiency in Fibonacci generator on the scale of frequency 1GHz and 10GHz. Therefore, LVDCI-DC2 I/O standard can be used to optimize power Dissipation for 1GHz frequency and SSTL can be used to optimize Power dissipation on 10GHz frequency.

References

[1] 7 Series FPGA SelectIO Resources User Guide UG361 (v1.4) June 21, **2013**. http://japan.xilinx.com/support/documentation/user_guides/ug471_7Series_SelectIO.pdf

[2] Sumita Nagah, and B. Pandey, "SSTL IO Standard Based Green Communication Using Fibonacci Generator Design on Ultra Scale FPGA", IEEE International Conference on Green Computing and Engineering Technology (ICGCET), **2015**.

[3] B. Pandey, and R. Kumar , "Low Voltage DCI Based Low Power VLSI Circuit Implementation on FPGA", IEEE Conference on Information and Communication Technologies(ICT), **2013**.

[4] B. Pandey, et. al. "Energy Efficient Design and Implementation of ALU on 40-nm FPGA", IEEE Conference on Energy Efficient Technologies for Sustainability-(ICEETs), **2013**.

[5] P. Kannan, K.S. Raghunathan, S. Jayaraman, "Aspects and solutions to designing standard LVCMOS I/O buffers in 90nm process", AFRICON 2007, pp. 1-7, **2007**

[6] P. Kannan, "Fundamental blocks of single ended LVCMOS output buffer- a circuit level design guideline", 18th European Conference on Circuit Theory and Design, pp. 392- 395, **2007**

[7] S. Goonatilake, "Toward a Global Science", Indiana University Press, p. 126, ISBN 978-0-253-33388-9, **1998**.

[8] P. Singh , "The So-called Fibonacci numbers in ancient and medieval India", Historia Mathematica, pp: 229–44, **1985**.

[9] T. Kumar, B. Pandey, T. Das, M.A. Rahman "SSTL Based Green Image ALU Design on different FPGA", IEEE conference on Green Computing, Communication and Conservation of Energy(ICGCE), 12-14 December, **2013**

[10] T. Kumar, B. Pandey, T. Das, S. Dabas and P. Kumar "Simulation of Voltage Based Efficient Fire Sensor on FPGA Using SSTL IO Standards", IEEE Conference on Robotics & Emerging Allied Technologies in Engineering (iCREATE), **2014**.

